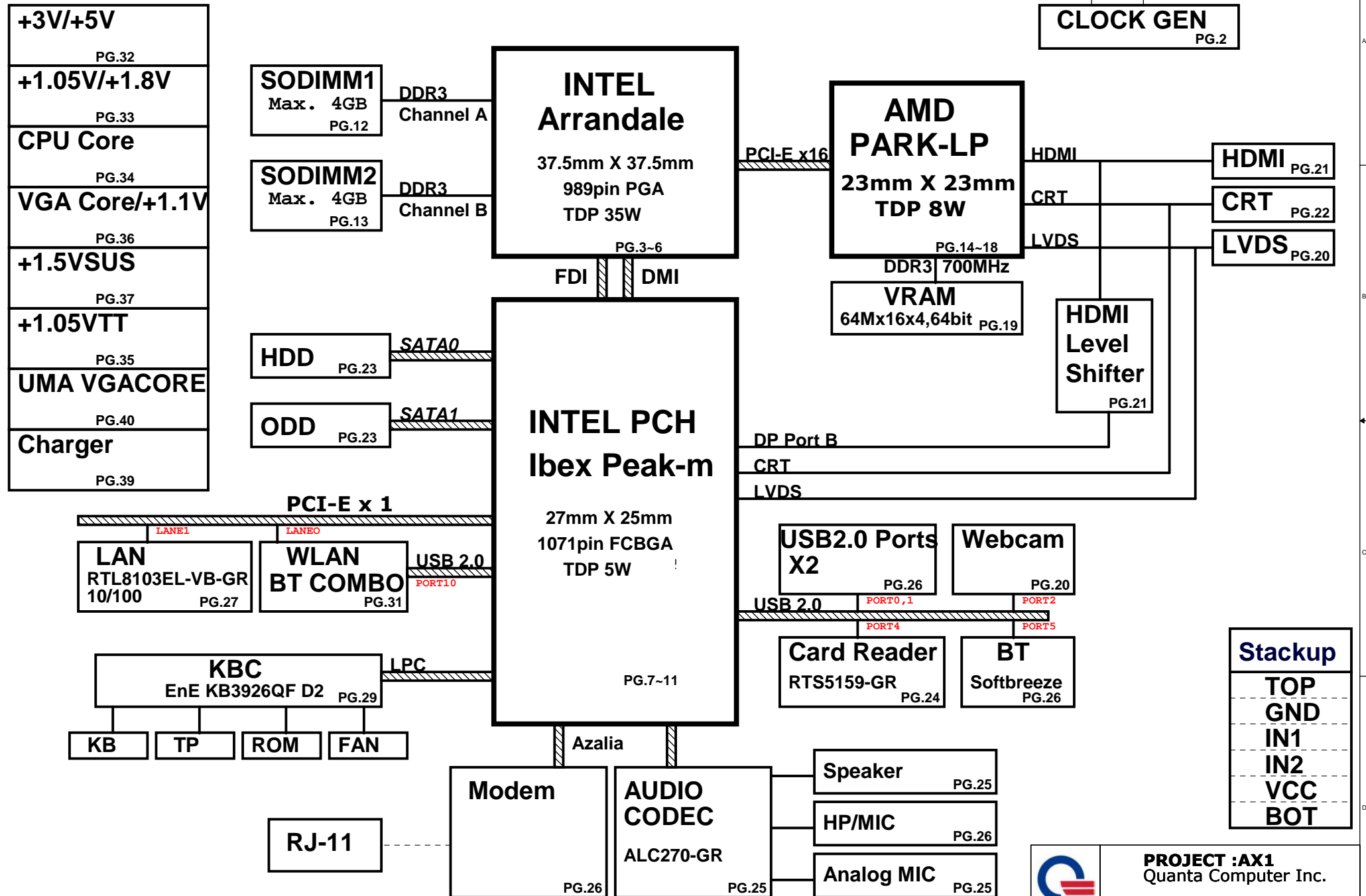
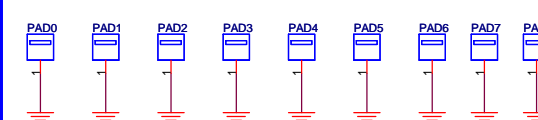
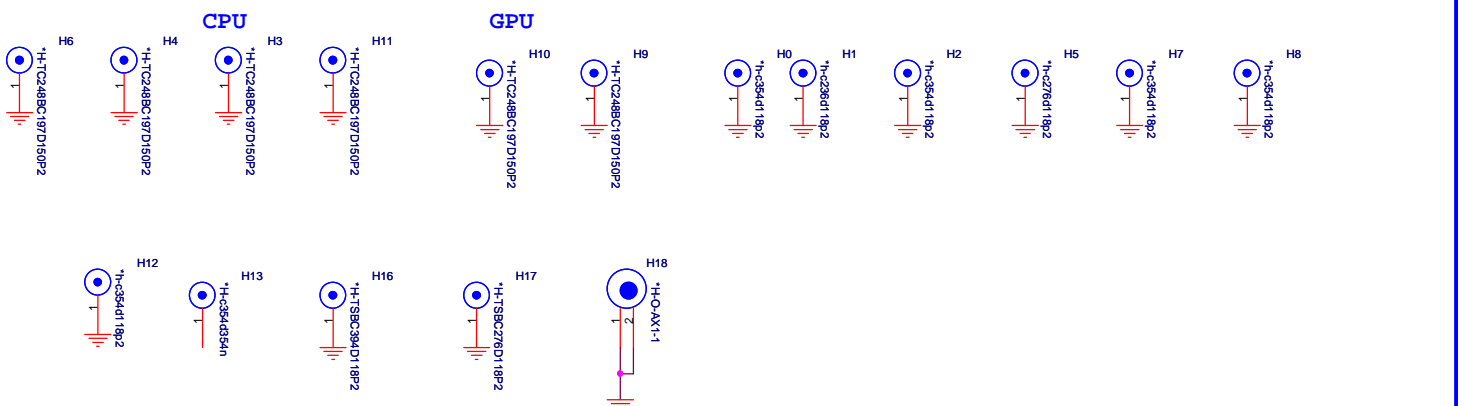
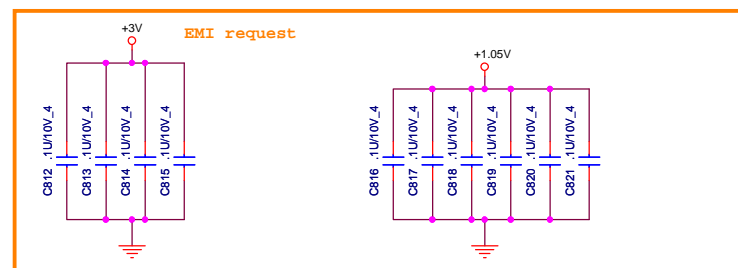
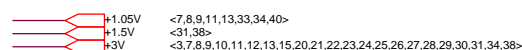
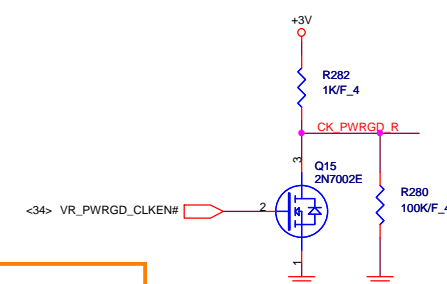
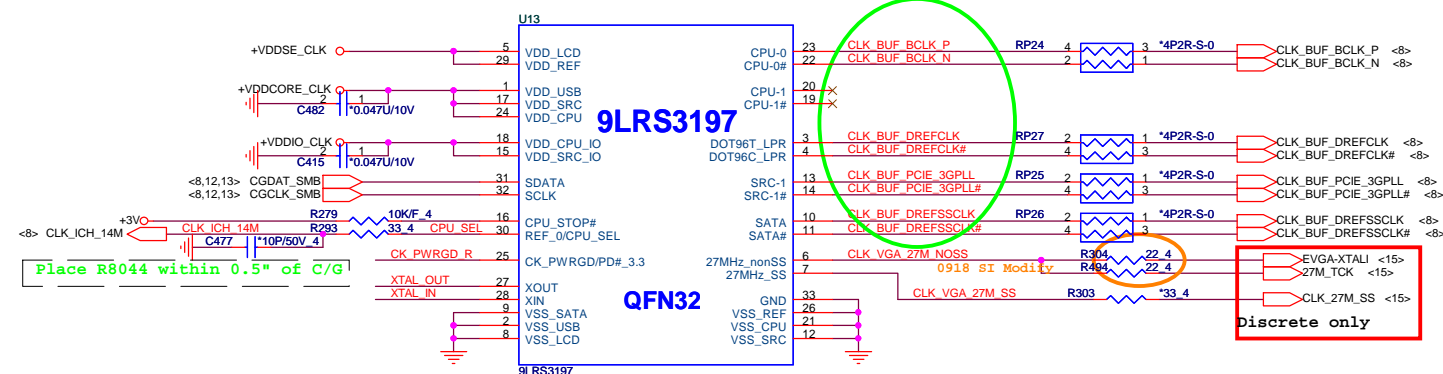
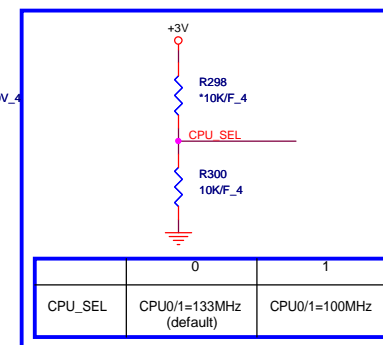
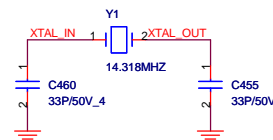
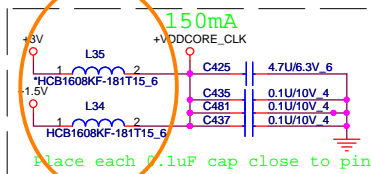


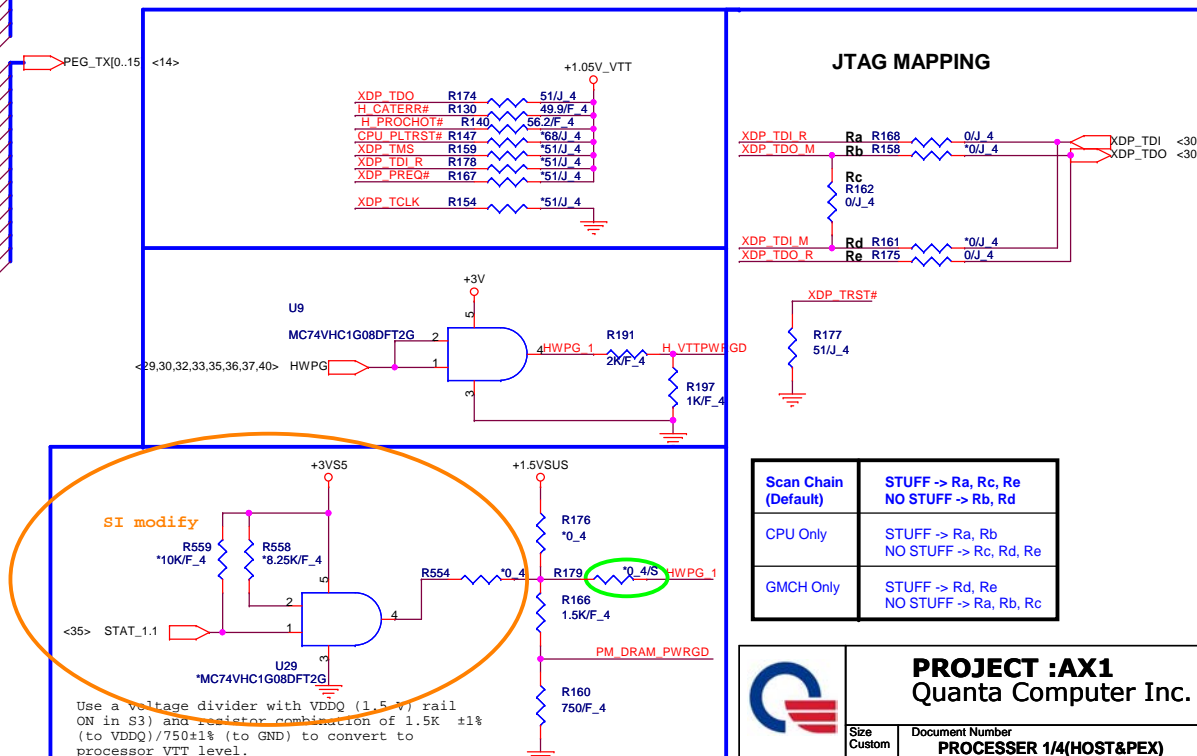
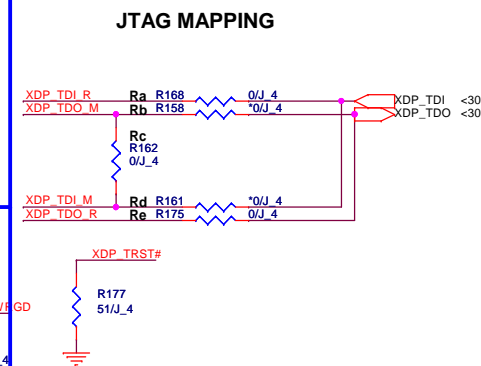
AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM





Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Size Custom	Document Number PROCESSER 1/4(HOST&PEX)
Date: Monday, November 30, 2009	Sheet 3 of 4



DDR SYSTEM MEMORY A

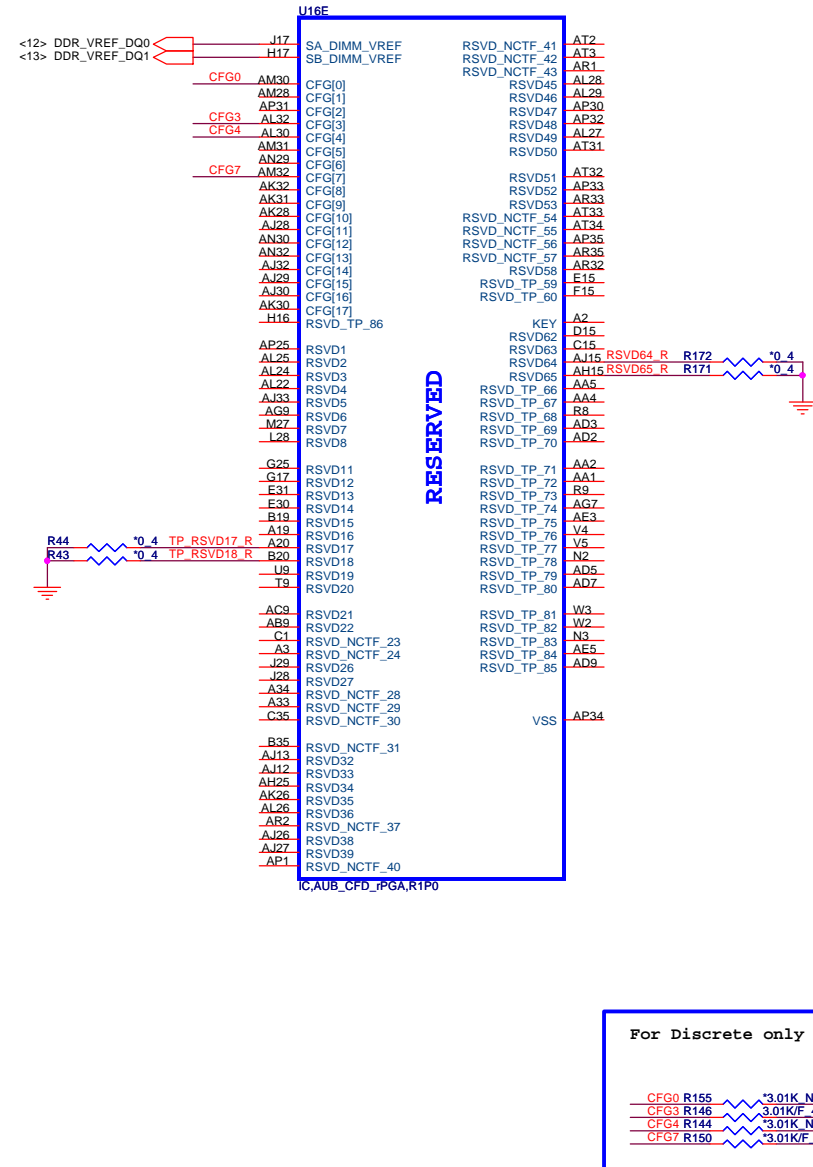
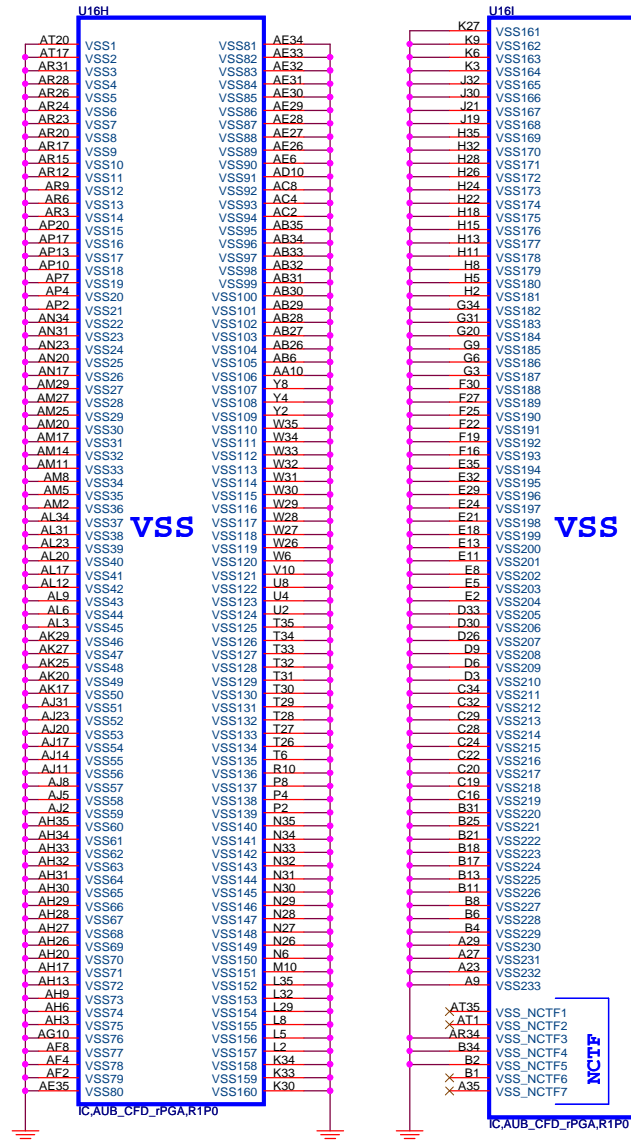
DDR SYSTEM MEMORY B

DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only.



AUBURNDAL/CLARKSFIELD PROCESSOR (GND)

AUBURNDAL/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



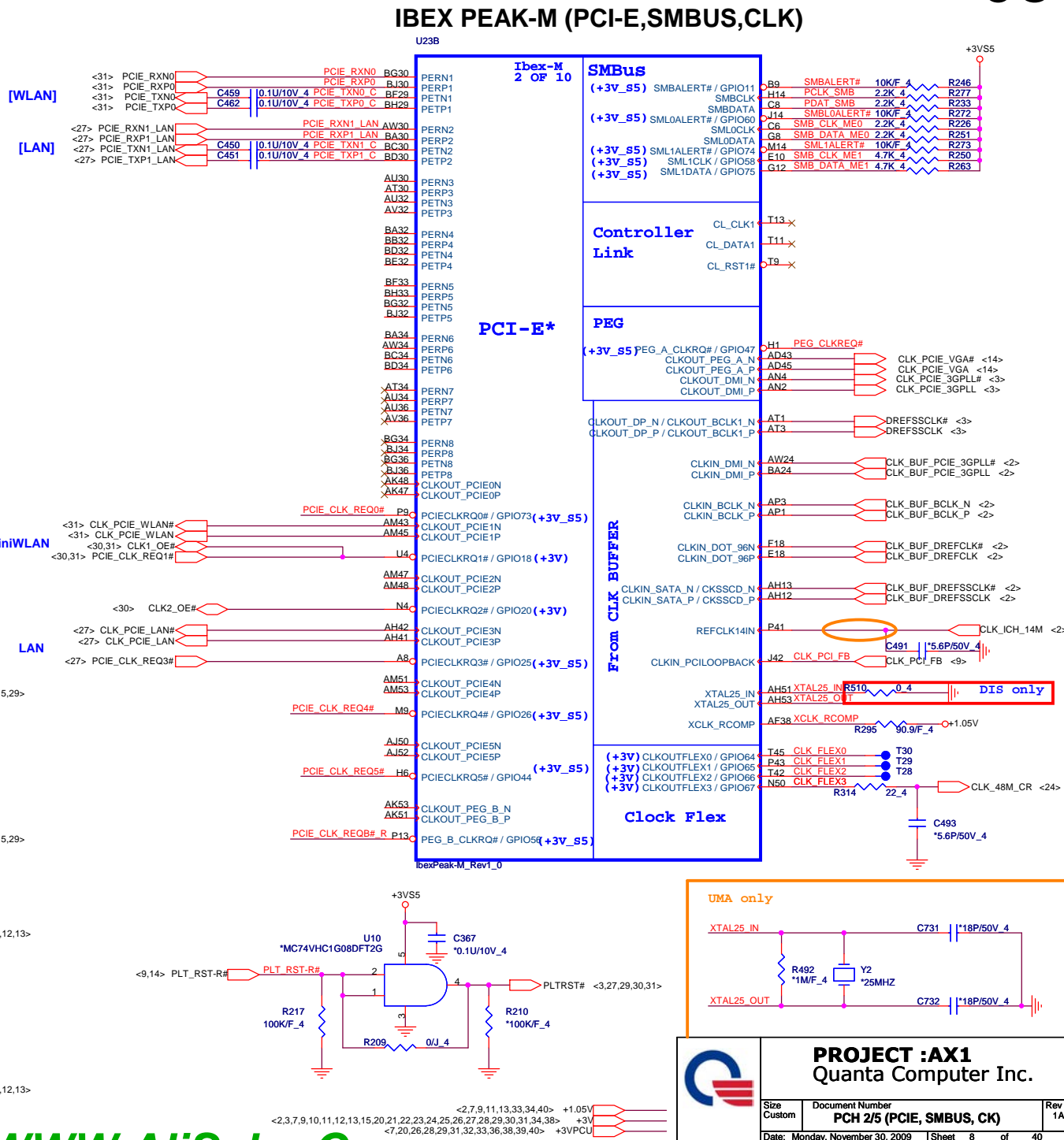
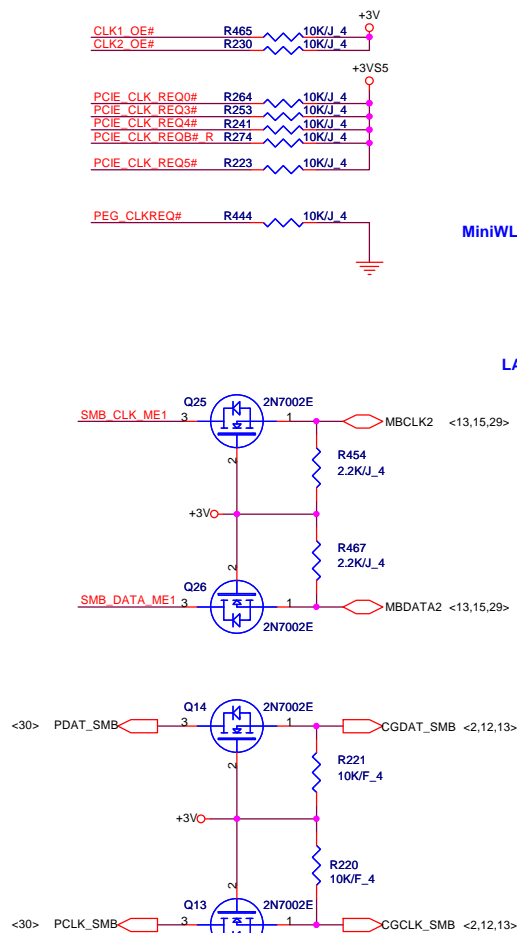
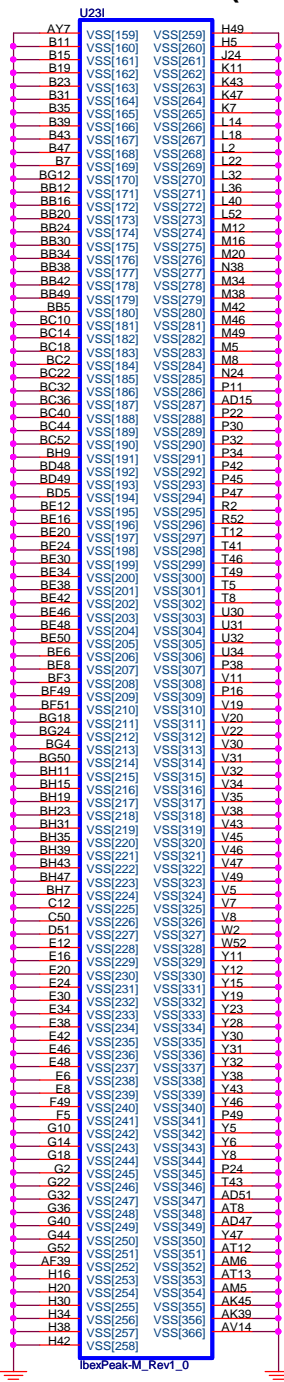
CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG



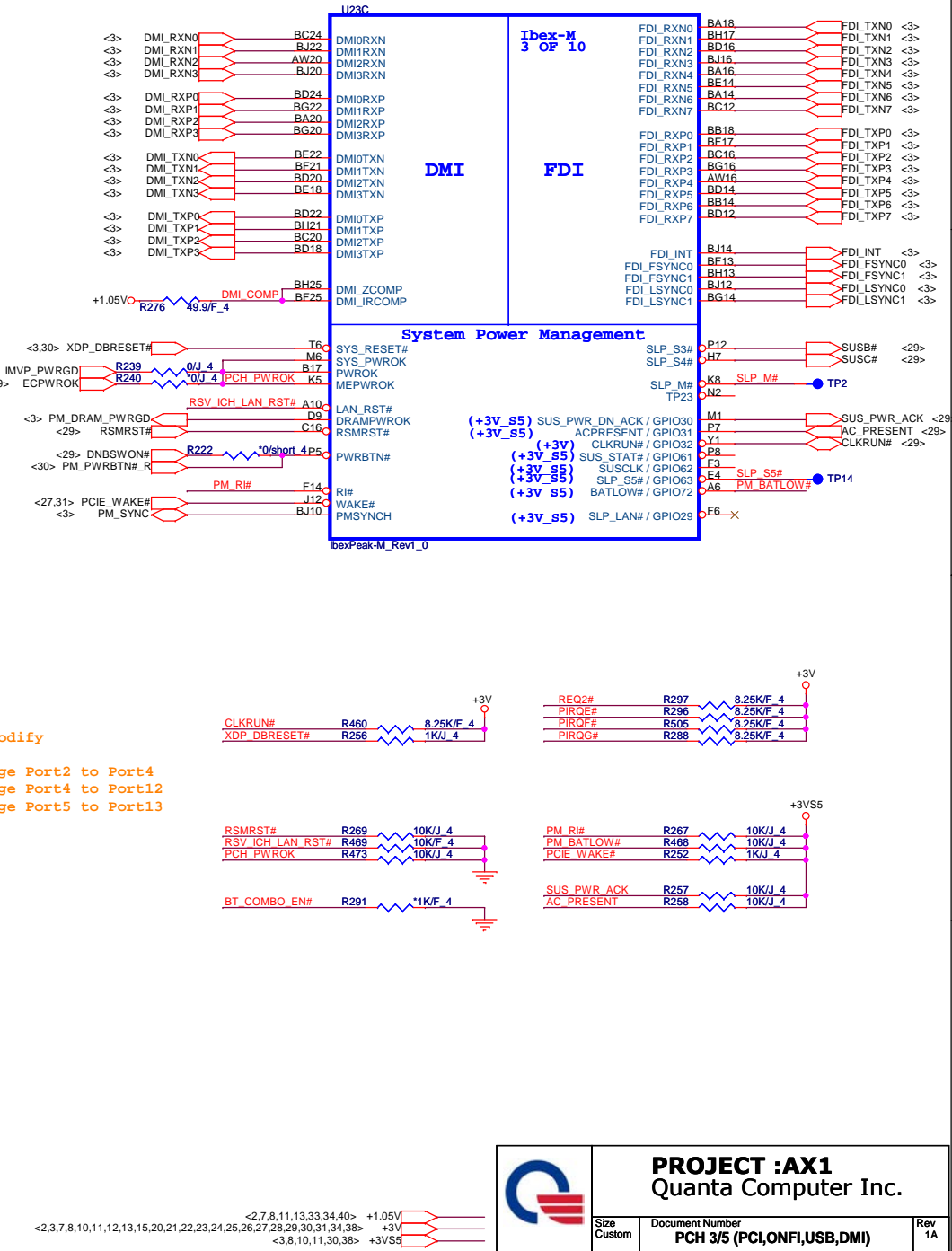
PROJECT :AX1
Quanta Computer Inc.

Size Custom Document Number
PROCESSOR 4/4 (GND)
 Date: Thursday, November 12, 2009 | Sheet 6 of 40

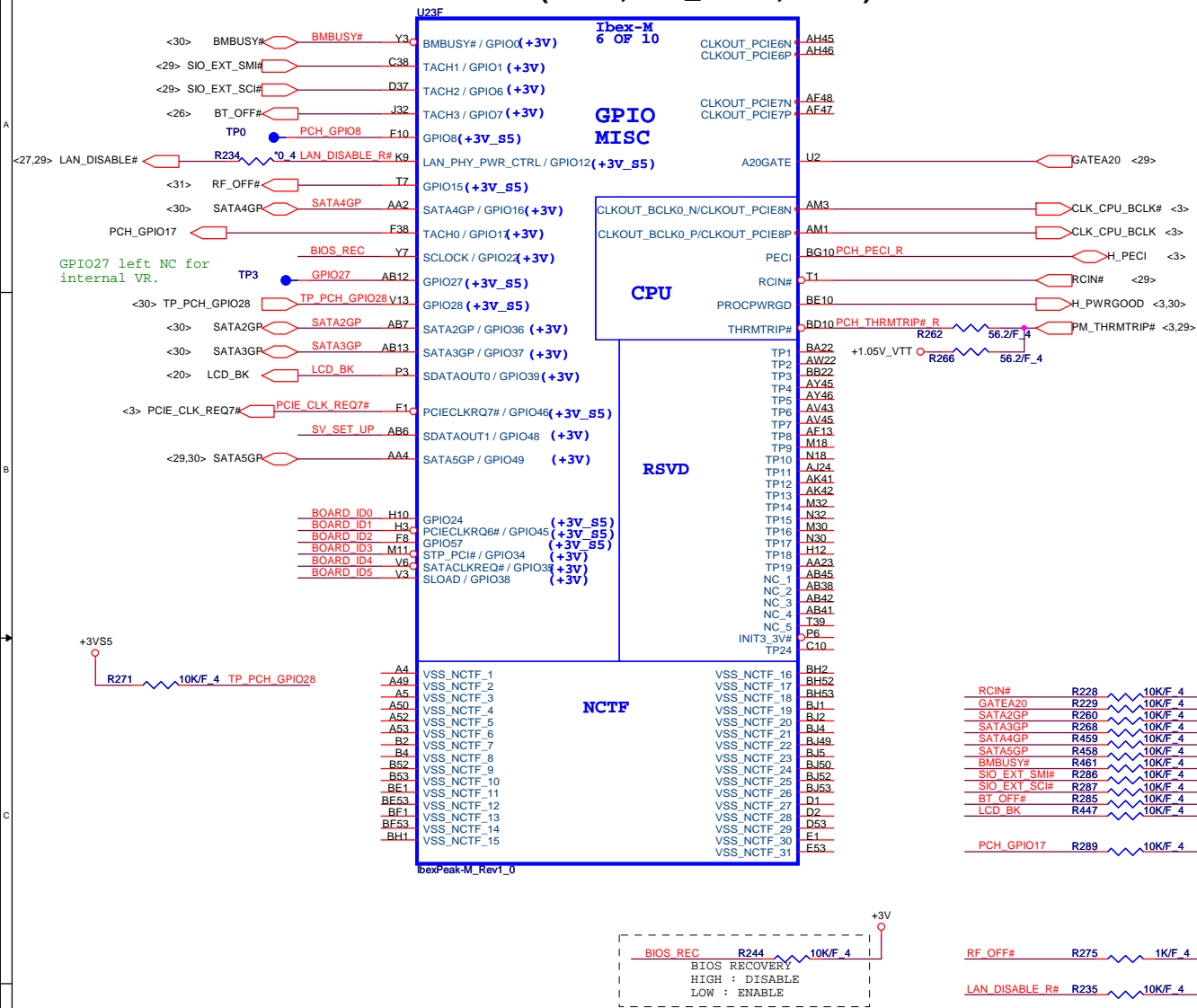
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



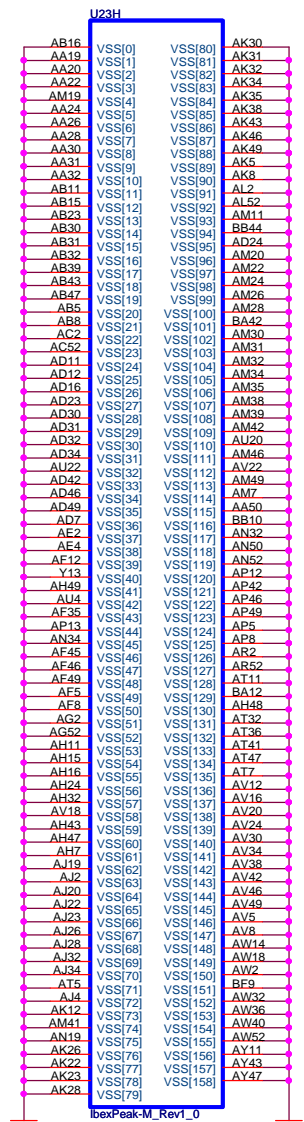
IBEX PEAK-M (PCI,USB,NVRAM)



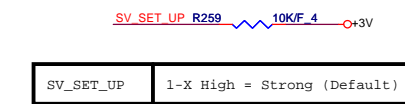
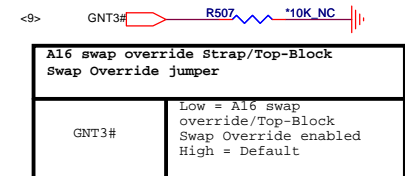
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

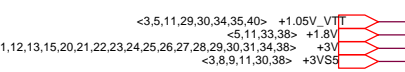
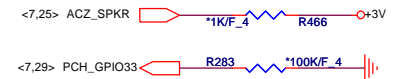


Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap



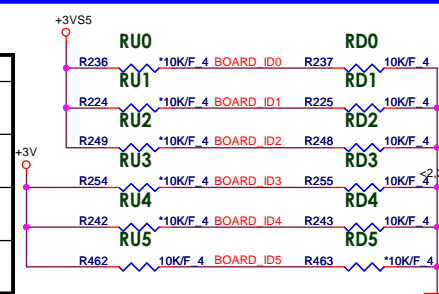
PROJECT :AX1
Quanta Computer Inc.

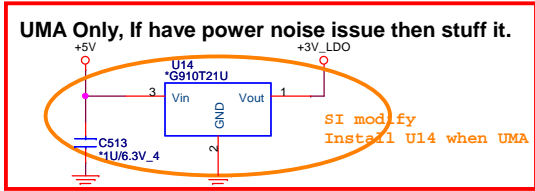
Size Custom Document Number PCH 4/5 (GPIO & Strap)
Date: Thursday, November 12, 2009 Sheet 10 of 40

BOARD ID SETTING

Board ID5: For identify UMA and DIS
Board ID4: For identify FF and DF
Board ID3: Reserve
Board ID2: Reserve
Board ID1: Reserve

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA FF	0	0	0	0	0	0
UMA DF	0	0	0	0	1	0
DIS	0	0	0	0	0	1





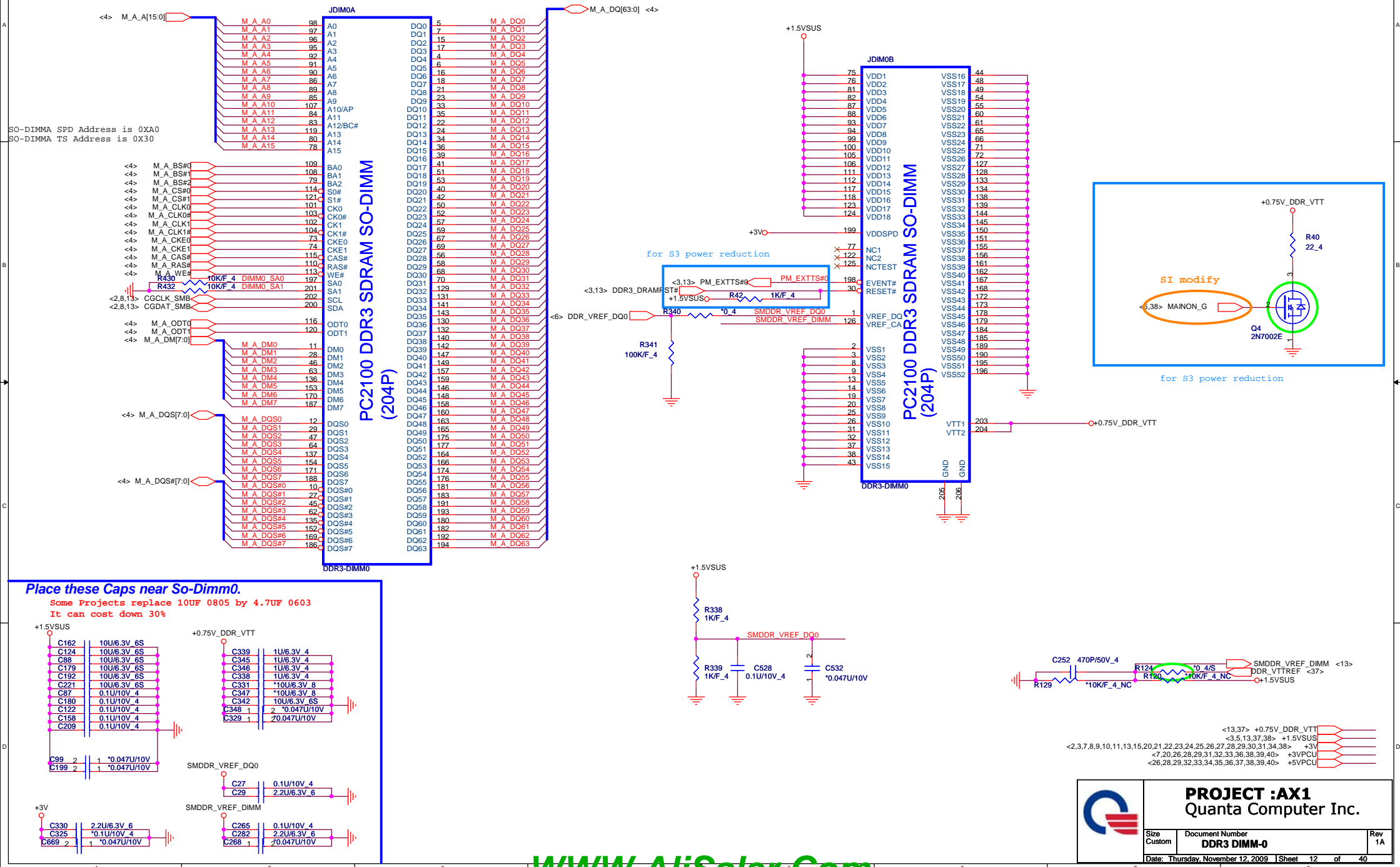
	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

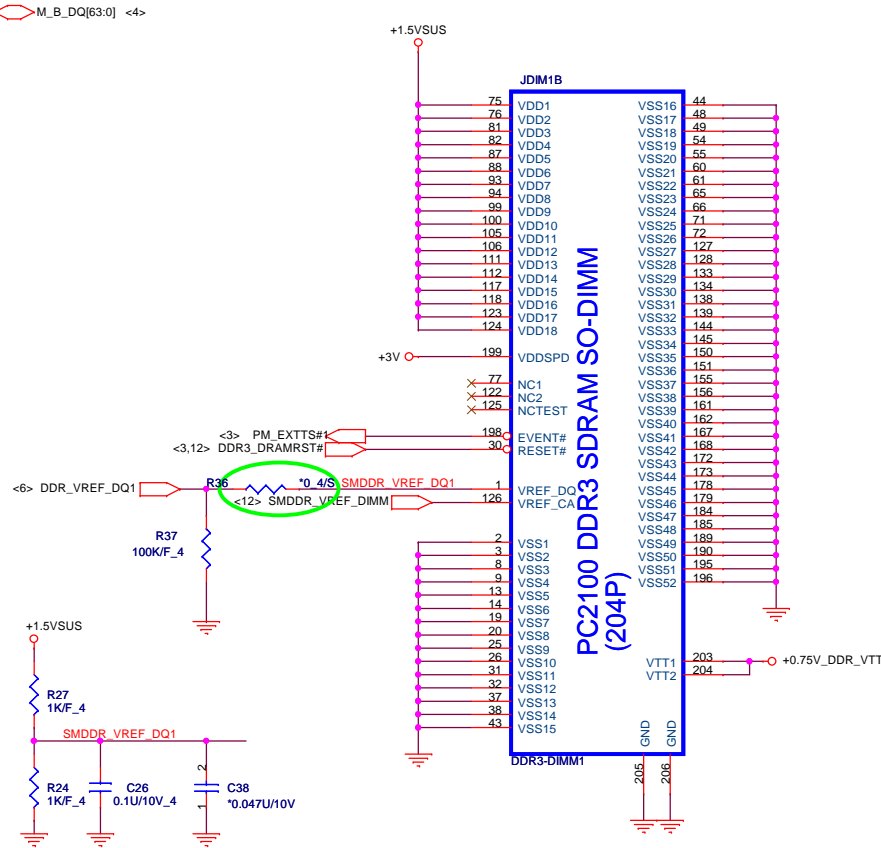
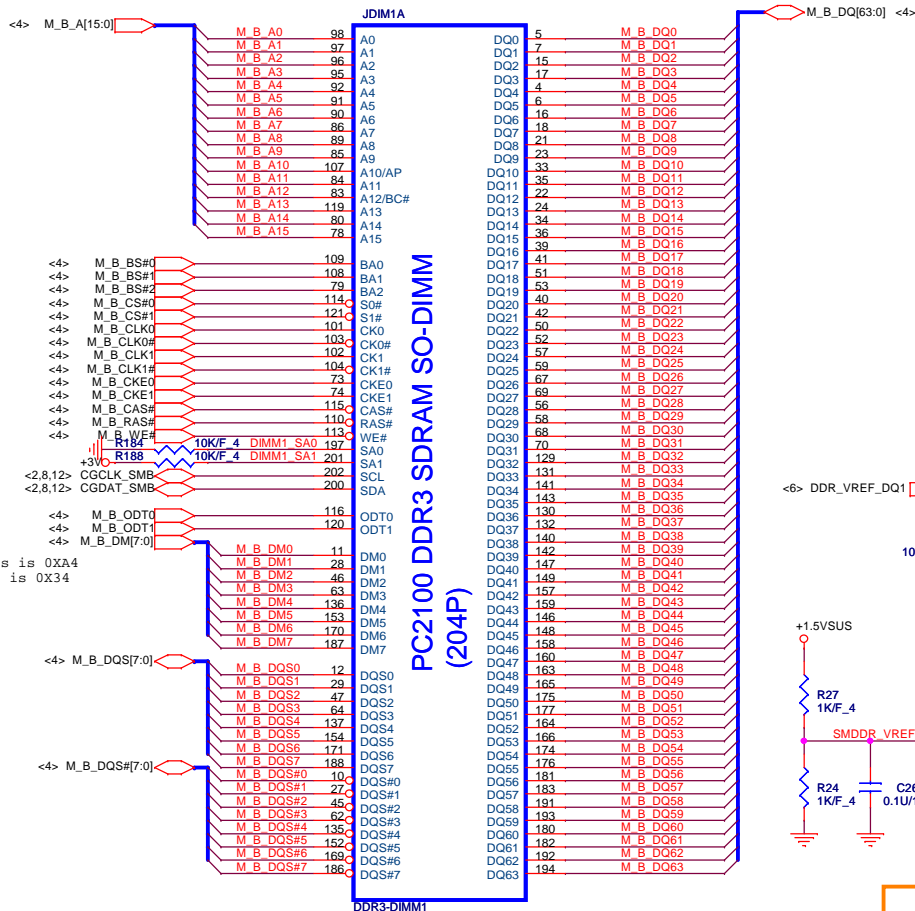
$\langle 2, 7, 8, 9, 13, 33, 34, 40 \rangle$ +1.05V
 $\langle 3, 5, 10, 29, 30, 34, 35, 40 \rangle$ +1.05V_VTT
 $\langle 5, 33, 38 \rangle$ +1.8V
 $\langle 2, 3, 7, 8, 9, 10, 12, 13, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 34, 38 \rangle$ +3V
 $\langle 3, 8, 9, 10, 30, 38 \rangle$ +3VS5
 $\langle 20, 21, 22, 23, 25, 28, 31, 38 \rangle$ +5V
 $\langle 32, 38 \rangle$ +5VS5



PROJECT :AX1
Quanta Computer Inc.

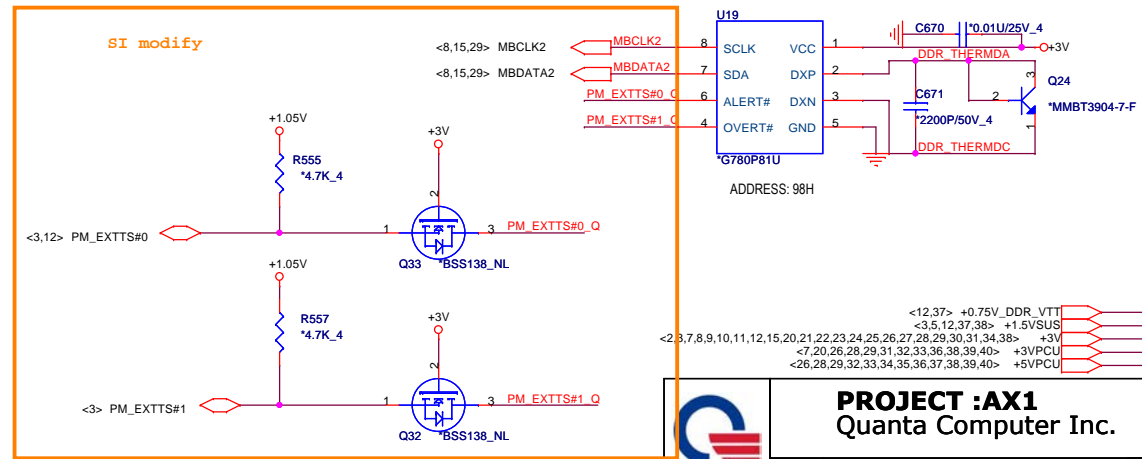
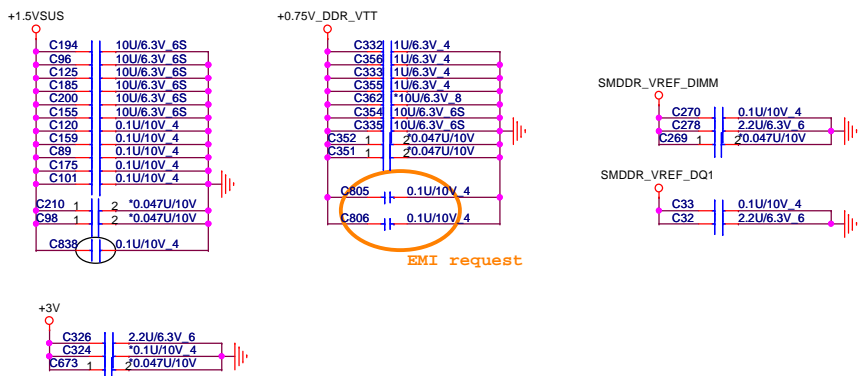
Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
Date: Thursday, November 12, 2009	Sheet 11 of 40	





Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

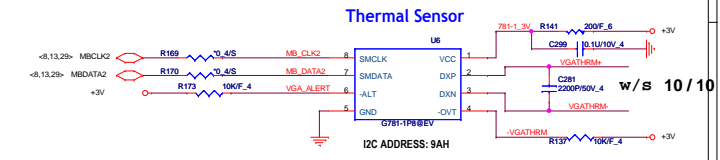
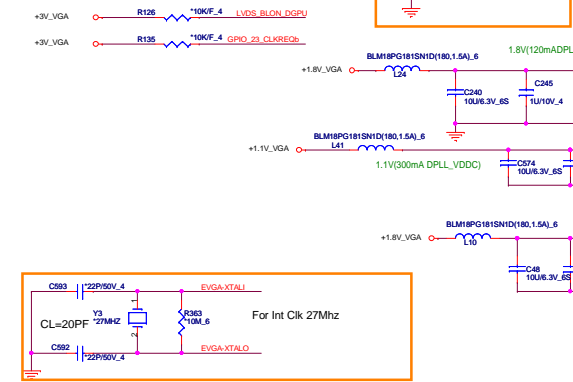
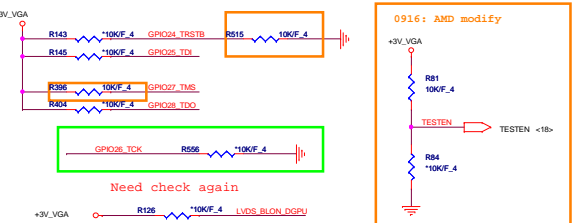
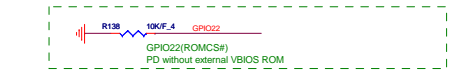
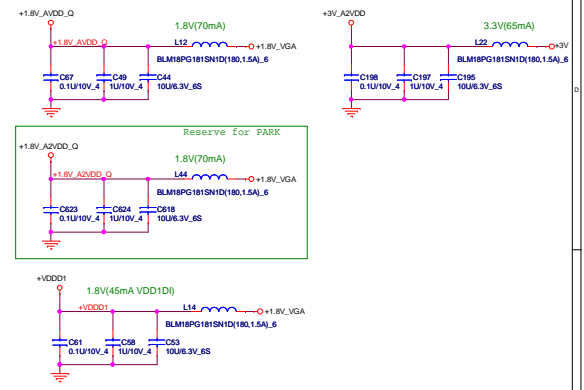
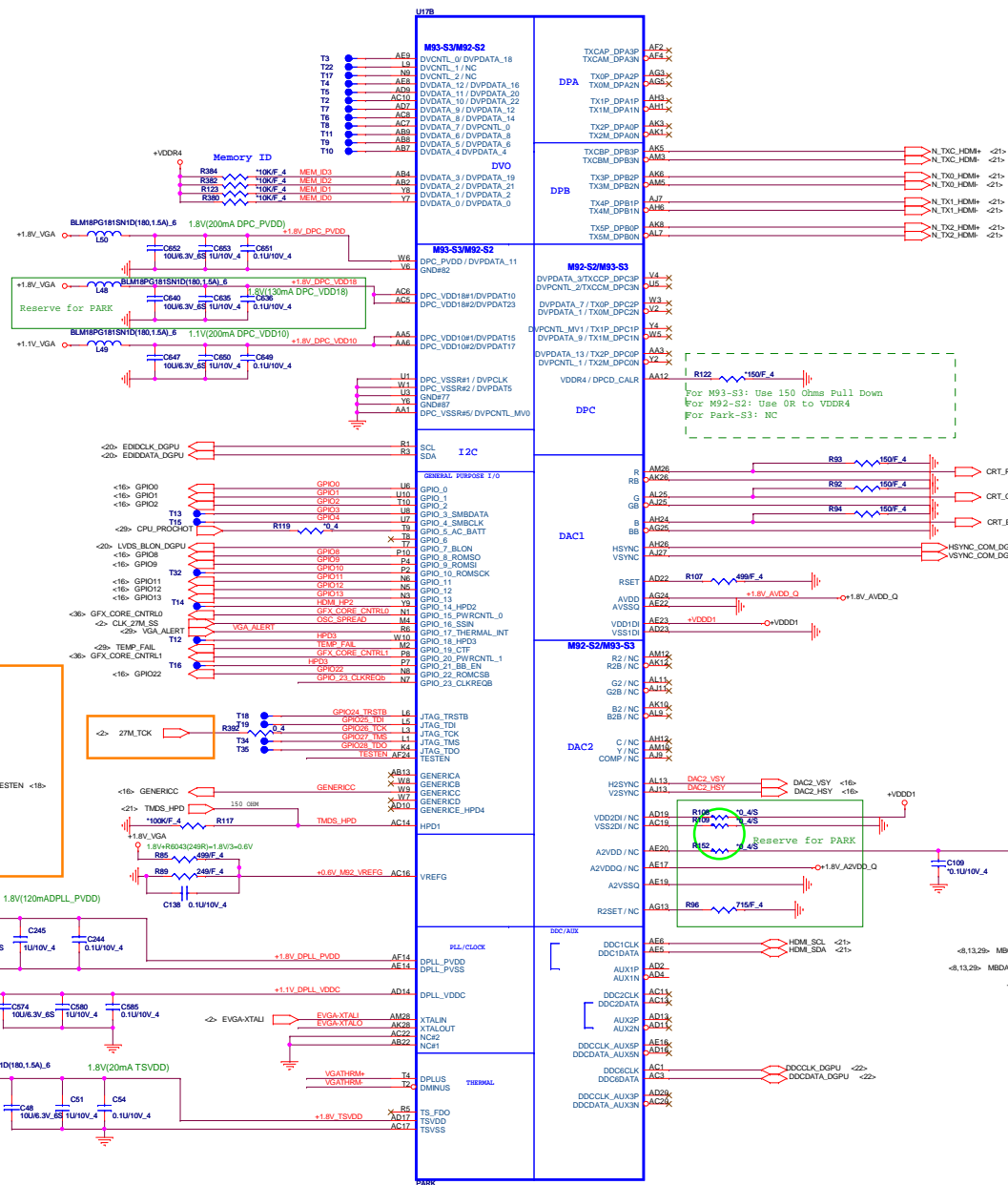



PROJECT :AX1
Quanta Computer Inc.

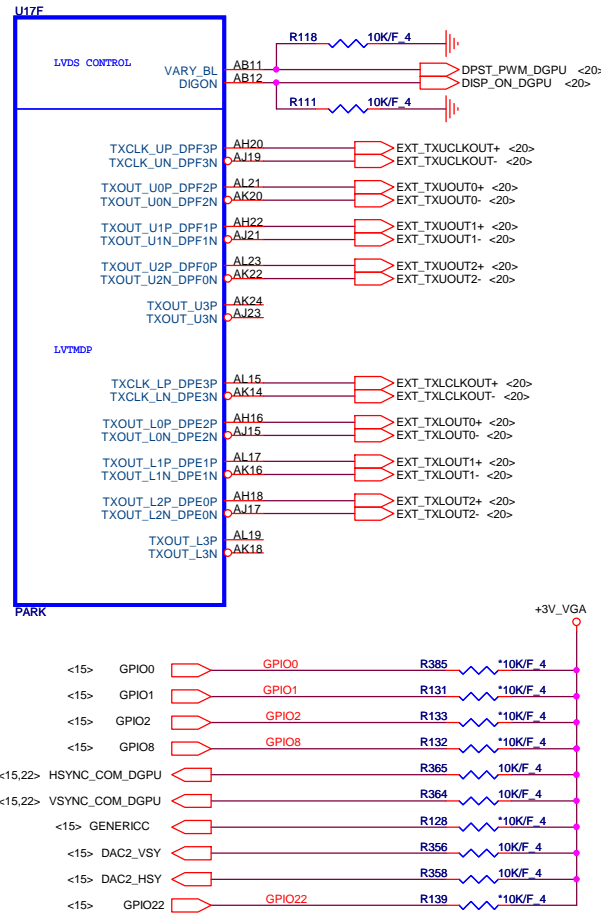
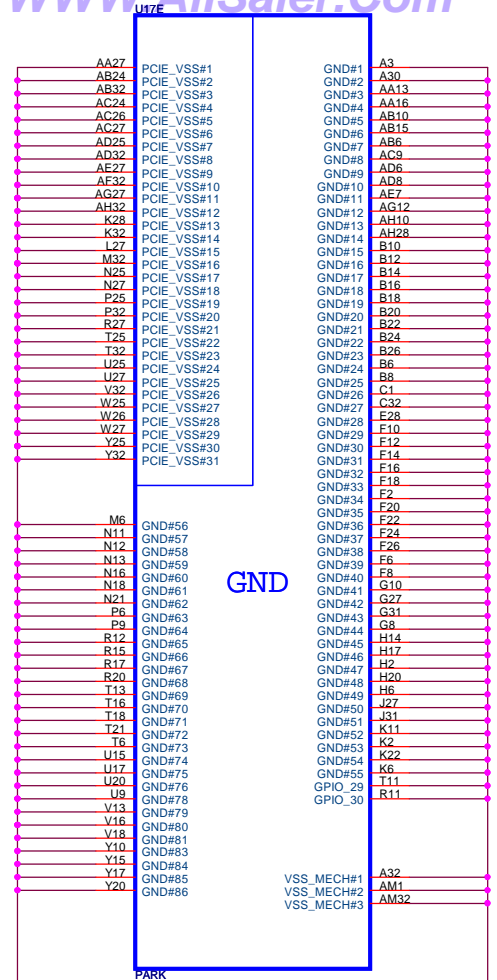
Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A
Date: Thursday, December 03, 2009	Sheet 13 of 40	



	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



	PROJECT :AX1 Quanta Computer Inc.		
	Size Custom	Document Number M93_MAIN	Rev 1A
	Date: Thursday, November 12, 2009 Sheet 15 of 40		



Memory Aperture size

GPI09		GPI013	GPI012	GPI011
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPI00	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPI02	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPI08 GPI09 GPI021	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPI0[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

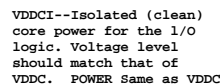
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPI021_BB_EN	

PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number M93_GND / LVDS / Straps	Rev 1A
Date: Thursday, November 12, 2009	Sheet 16 of 40	



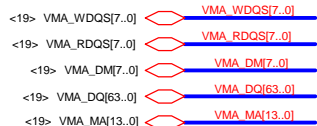
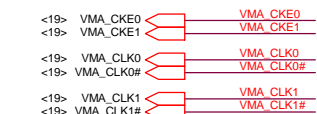
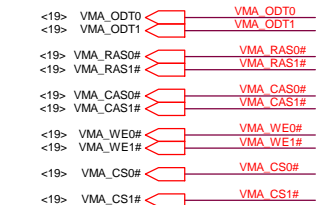
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V ($\pm 5\%$)

PCIE_VDDC--PCI-E
Digital Power
Supply (Either 1.0
V or 1.1 V) 1.0 V
-5% to 1.1 V +5%



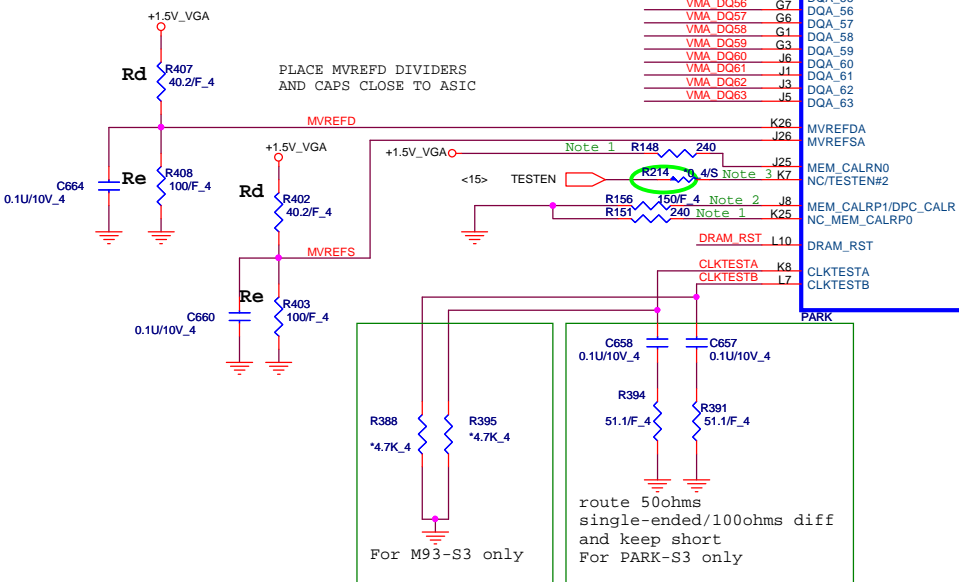
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number M93_Power_and_NC	Rev 1A
Date: Tuesday, November 10, 2009		Sheet 17 of 40

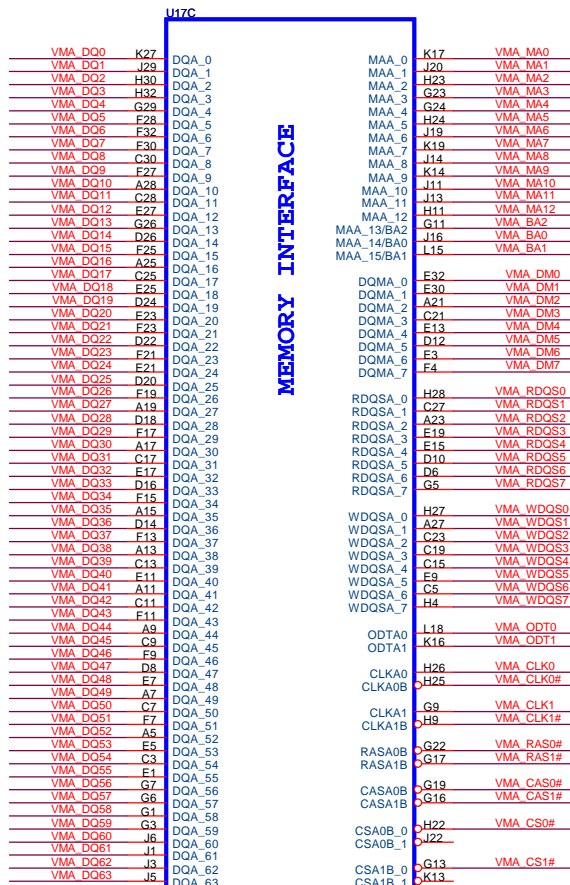


support 1gbit
VRAM (64M X 16)

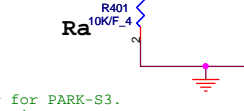
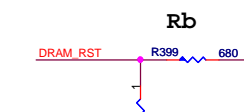
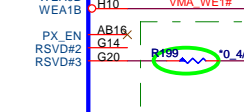
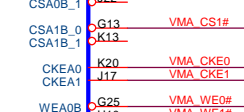
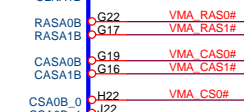
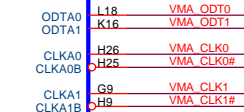
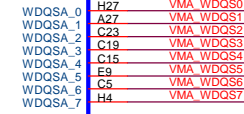
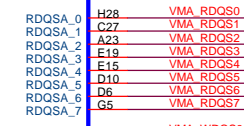
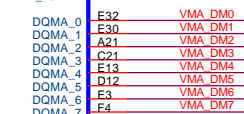
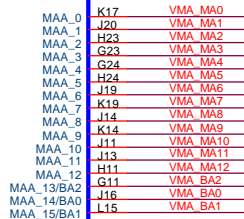
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Rd)	40.2R	40.2R
MVREF TO GND (Re)	100R	100R



Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
 Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
 For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
 Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
 For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



MEMORY INTERFACE



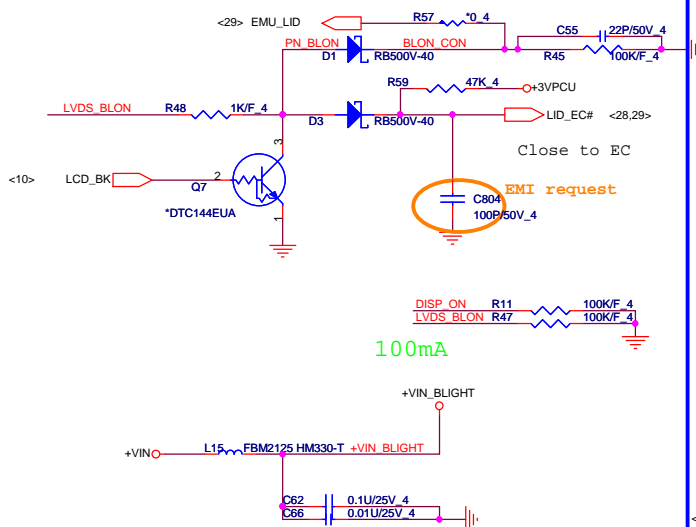
Designator	M9X-S2 and M93-S3	Park-S3
Ra	NC	10K
Rb	0R/Short	680R
Rc	2.2K	NC
Ca	2.2nF	68pF

PROJECT :AX1
Quanta Computer Inc.

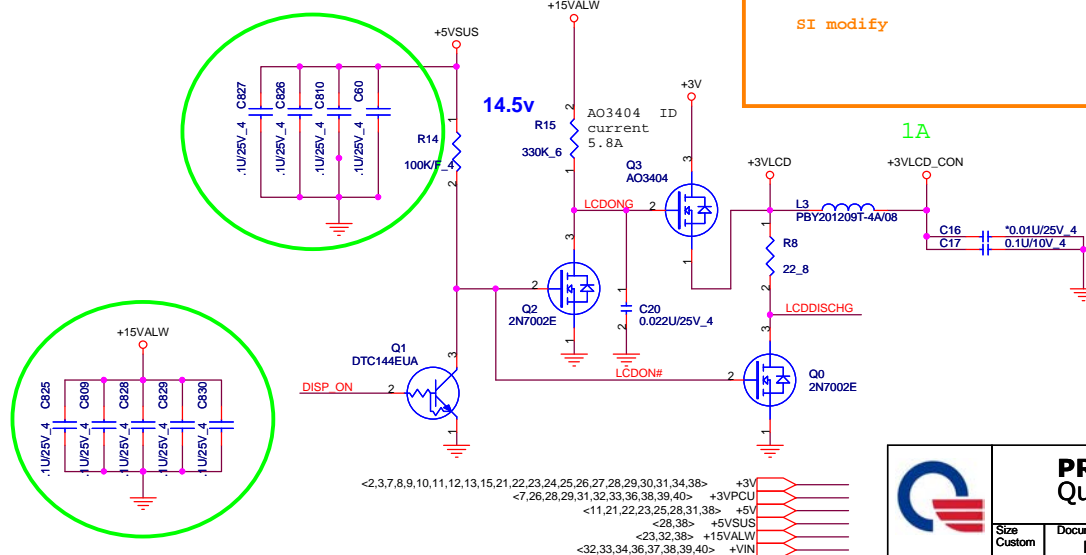
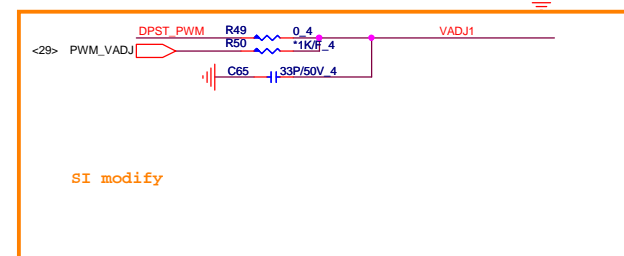
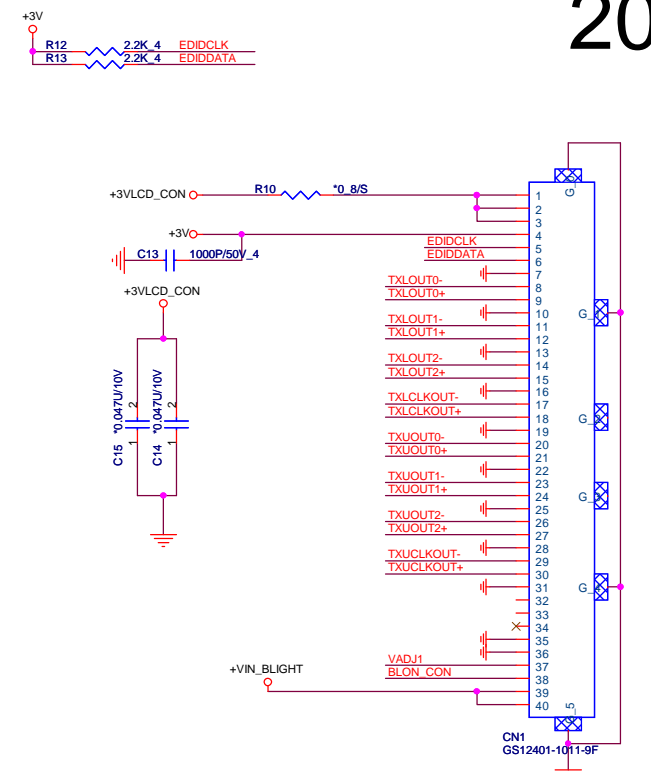
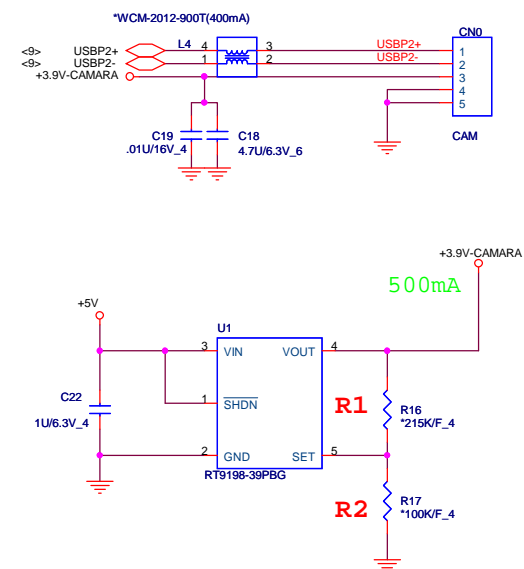
Size Custom	Document Number M93_MEM_Interface	Rev 1A
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LID Switch



CAMERA



9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004



EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage	
CFG1:CFG0=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1	VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0	VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1	VIL:<0.36V VOL:0.6V

For UMA HDMI function

POWER

CONTROL











GND

***PS8101**

EQUALIZATION SETTING

PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 25dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:>0.6V (Default)
 CFG1:CFG0=0:1 VIL:<0.36V VOL>0.55V

TXC HDMI+	*4P2R S-3	1		2	RP21	C TXC HDMI-
TXC HDMI+	*4P2R S-3	1		4	RP20	C TXC HDMI+
TX0 HDMI+	*4P2R S-3	3		1	RP20	C TX0 HDMI+
TX0 HDMI-	*4P2R S-3	3		2	RP20	C TX0 HDMI-
TX1 HDMI-	*4P2R S-3	1		2	RP19	C TX1 HDMI-
TX1 HDMI+	*4P2R S-3	3		4	RP19	C TX1 HDMI+
TX2 HDMI+	*4P2R S-3	1		4	RP18	C TX2 HDMI+
TX2 HDMI-	*4P2R S-3	3		2	RP18	C TX2 HDMI-
HDMI SCLK R	*4P2R S-3 33	3		4	RP22	HDMI SCLK
HDMI SDATA R						HDMI SDATA

	PLACE	CLOSE	HDMI	CONN
<15> N_TX2_HDMI+	C177	0.1U/10V_4	C	TX2 HDMI+
<15> N_TX2_HDMI-	C172	0.1U/10V_4	C	TX2 HDMI-
<15> N_TX1_HDMI+	C168	0.1U/10V_4	C	TX1 HDMI+
<15> N_TX1_HDMI-	C169	0.1U/10V_4	C	TX1 HDMI-
<15> N_TX0_HDMI+	C150	0.1U/10V_4	C	TX0 HDMI+
<15> N_TX0_HDMI-	C141	0.1U/10V_4	C	TX0 HDMI-

The diagram shows a circuit for a 100kF 4.7V electrolytic capacitor (C18). The capacitor is connected to a +5V supply and a network of resistors (R379-R386) which are connected to various HDMI pins (C_TX2+ to C_TXC-). A 100kF 4.7V resistor (R77) is also shown in the circuit.

Resistor values and connections:

- R379: 499F_4 C_TX2+ HDMI+
- R378: 499F_4 C_TX2- HDMI+
- R375: 499F_4 C_TX1+ HDMI+
- R372: 499F_4 C_TX1- HDMI+
- R370: 499F_4 C_TX0+ HDMI+
- R369: 499F_4 C_TX0- HDMI+
- R368: 499F_4 C_TXC+ HDMI+
- R366: 499F_4 C_TXC- HDMI+

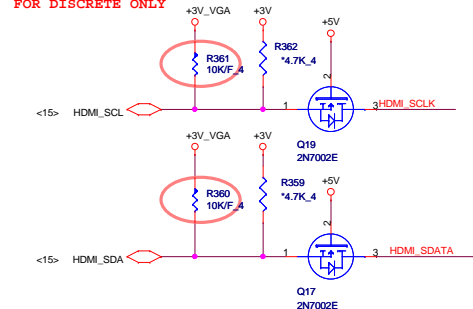
Capacitor: C18, 100kF_4.7V

Resistor: R77, 100kF_4.7V

Supply: +5V

SI model: SI model

FOR DISCRETE ONLY



UMA use +3V for the detect pin
Dis use +3V_VGA for the detect pin

<1> TMDS_HPD

Q6 MMIO3904-F

HDMI_DET

HDMI_DET

200K_F_4

200K_F_4

R62 0.4

R63 0.4

R64 10K_F_4

R72

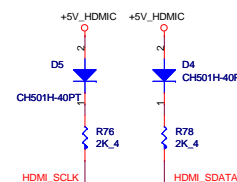
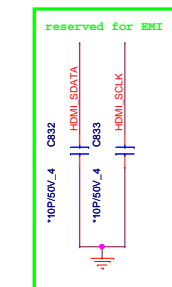
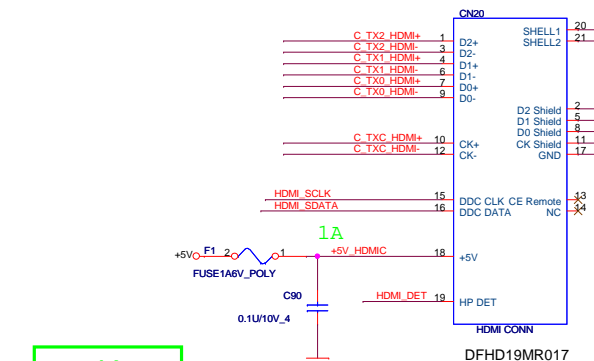
R71

+3V

+3V_VGA

C TX2 HDMI+	R561	*100F/4	C TX2 HDMI-
C TX1 HDMI+	R562	*100F/4	C TX1 HDMI-
C TX0 HDMI+	R563	*100F/4	C TX0 HDMI-
C TXC HDMI+	R564	*100F/4	C TXC HDMI-

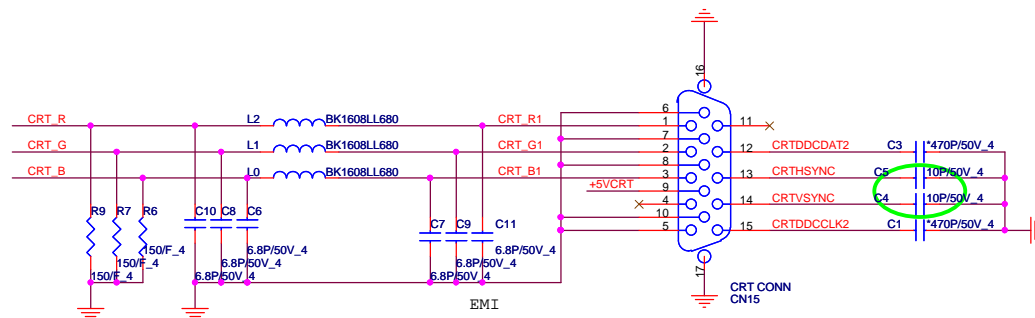
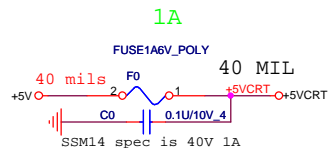
PV EMI request



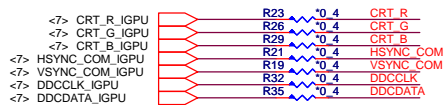
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number HDMI CONN	Rev 1A
Date: Monday, November 16, 2009	Sheet 21 of 40	

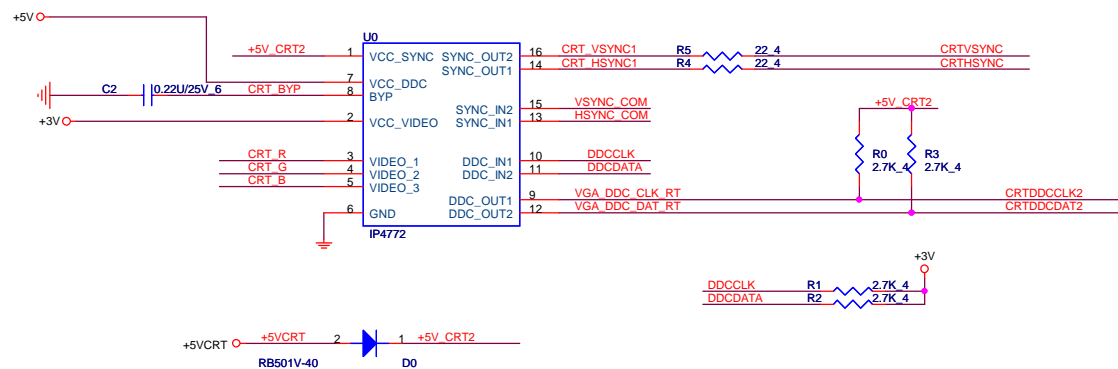
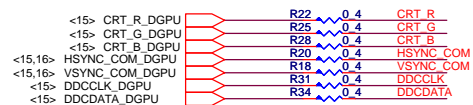
CRT PORT

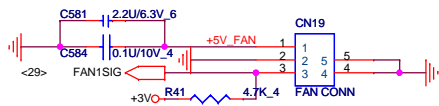


FOR UMA

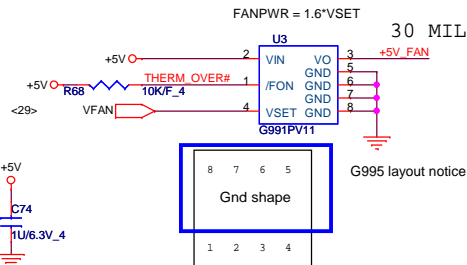


FOR DISCRETE

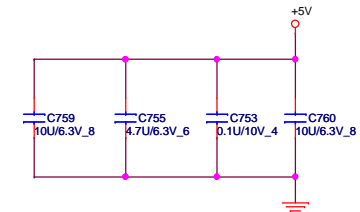
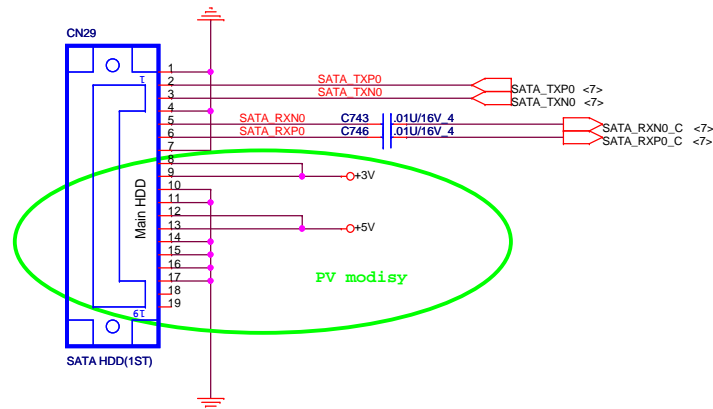




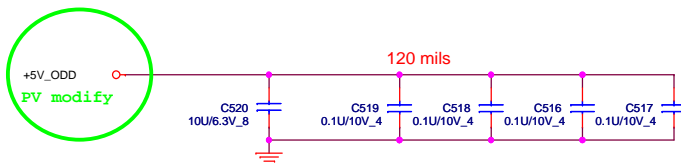
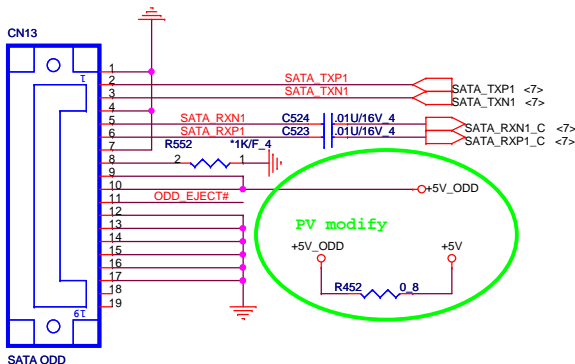
DFHD03MR008



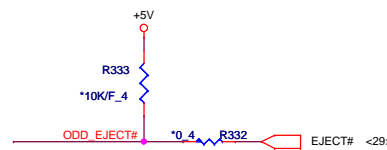
SATA HDD CONNECTOR



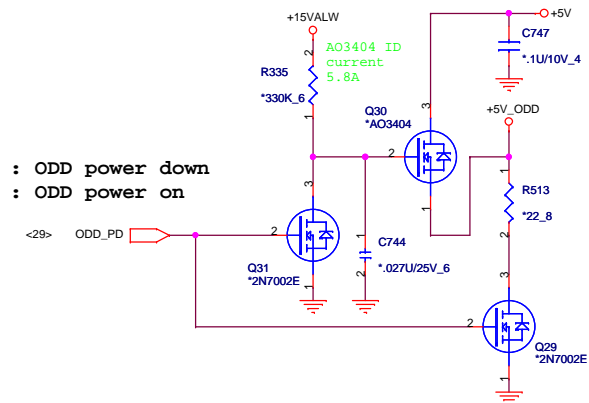
SATA ODD CONNECTOR



SI Add

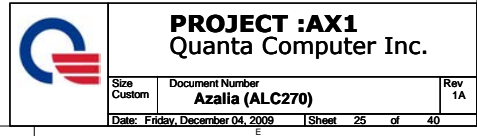


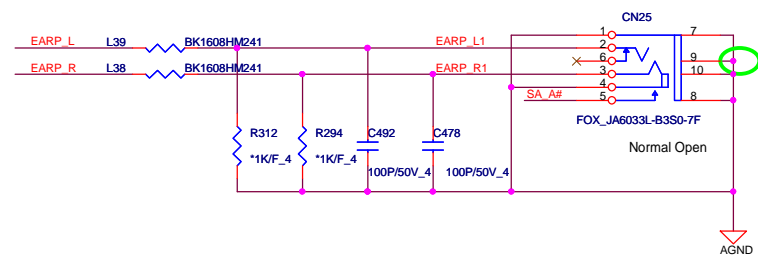
High : ODD power down
Low : ODD power on



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A
Date:	Thursday, November 12, 2009	Sheet 23 of 40

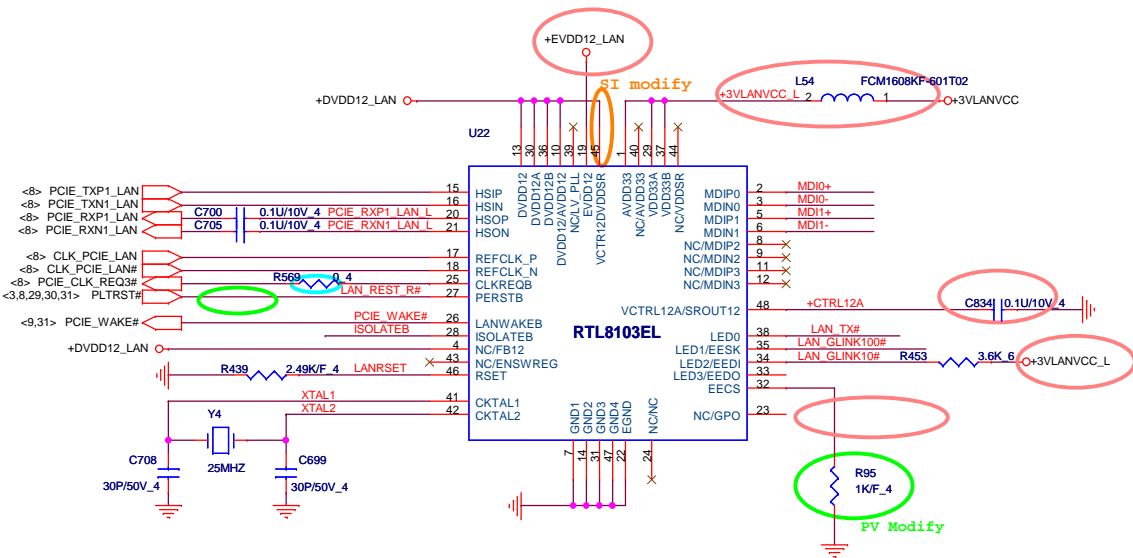




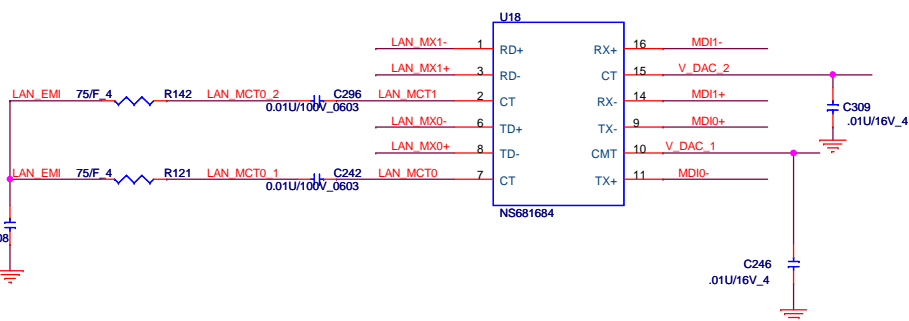
MIC



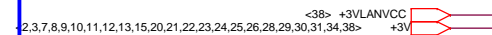
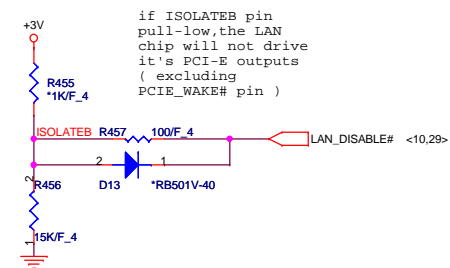
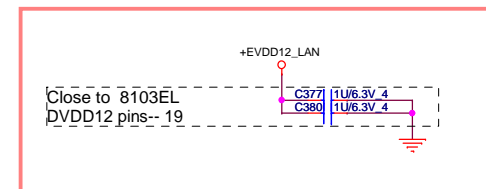
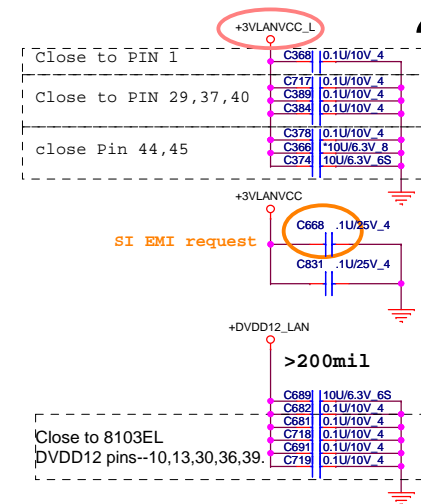
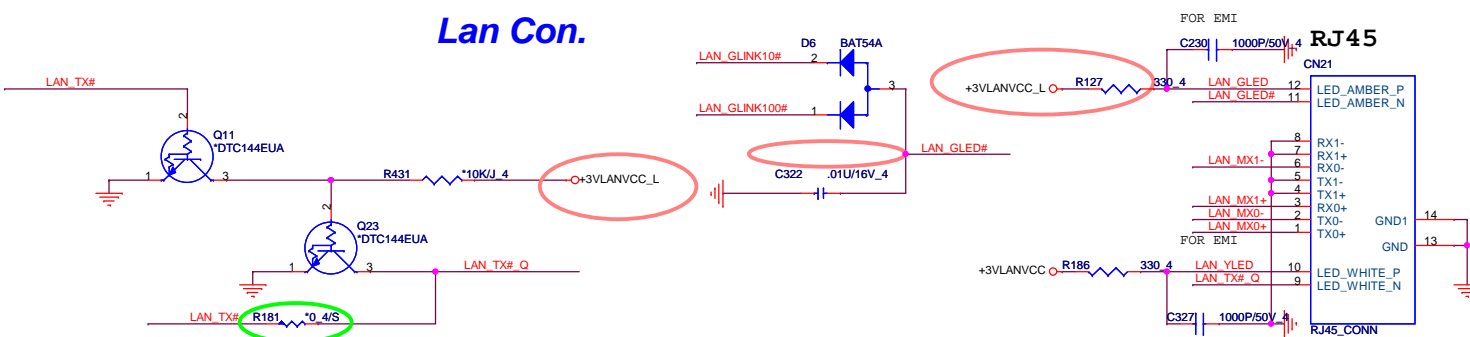
Size Custom	Document Number USB/BT/Modem/Audio Jack	Rev 1A
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Transformer for 10/100

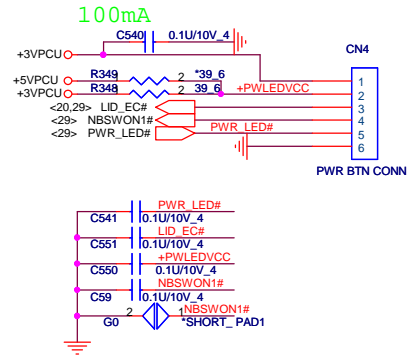


Lan Con.

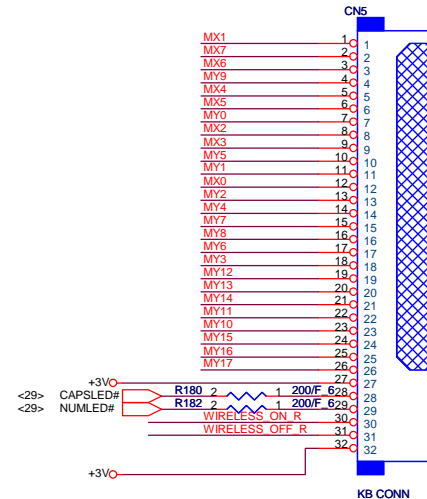
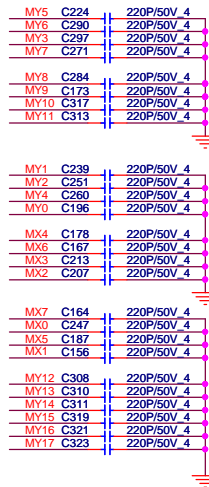


PROJECT :AX1
Quanta Computer Inc.

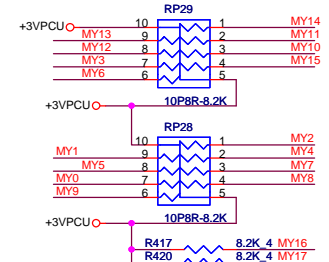
Size Custom	Document Number RTL8111DL/8103EL	Rev 1/
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KEYBOARD Con.

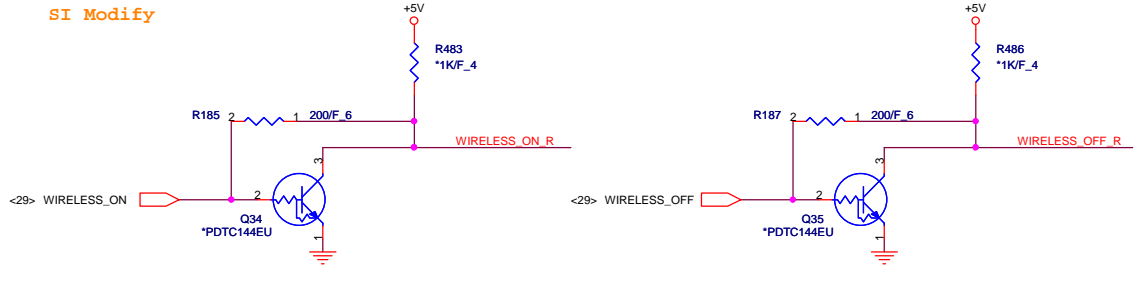


KEYBOARD PULL-UP

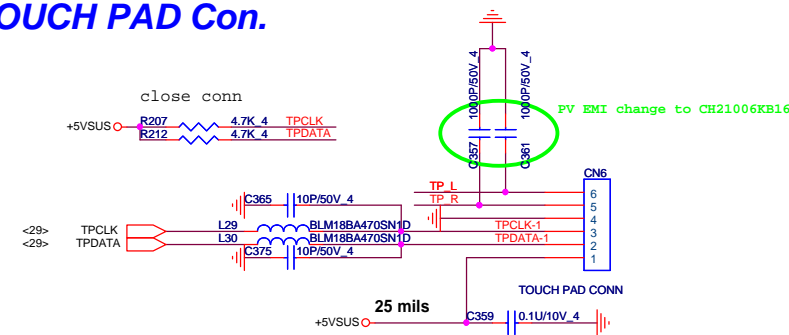


28

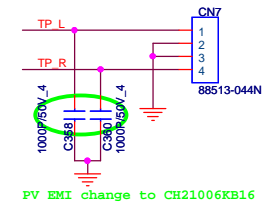
SI Modify



TOUCH PAD Con.

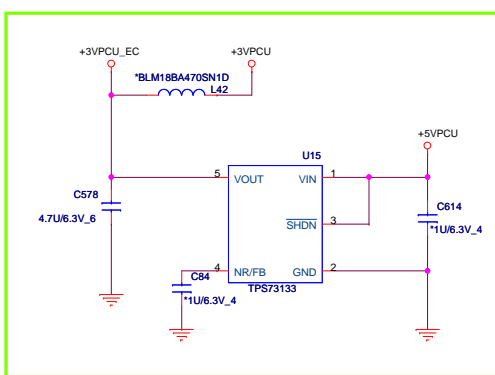
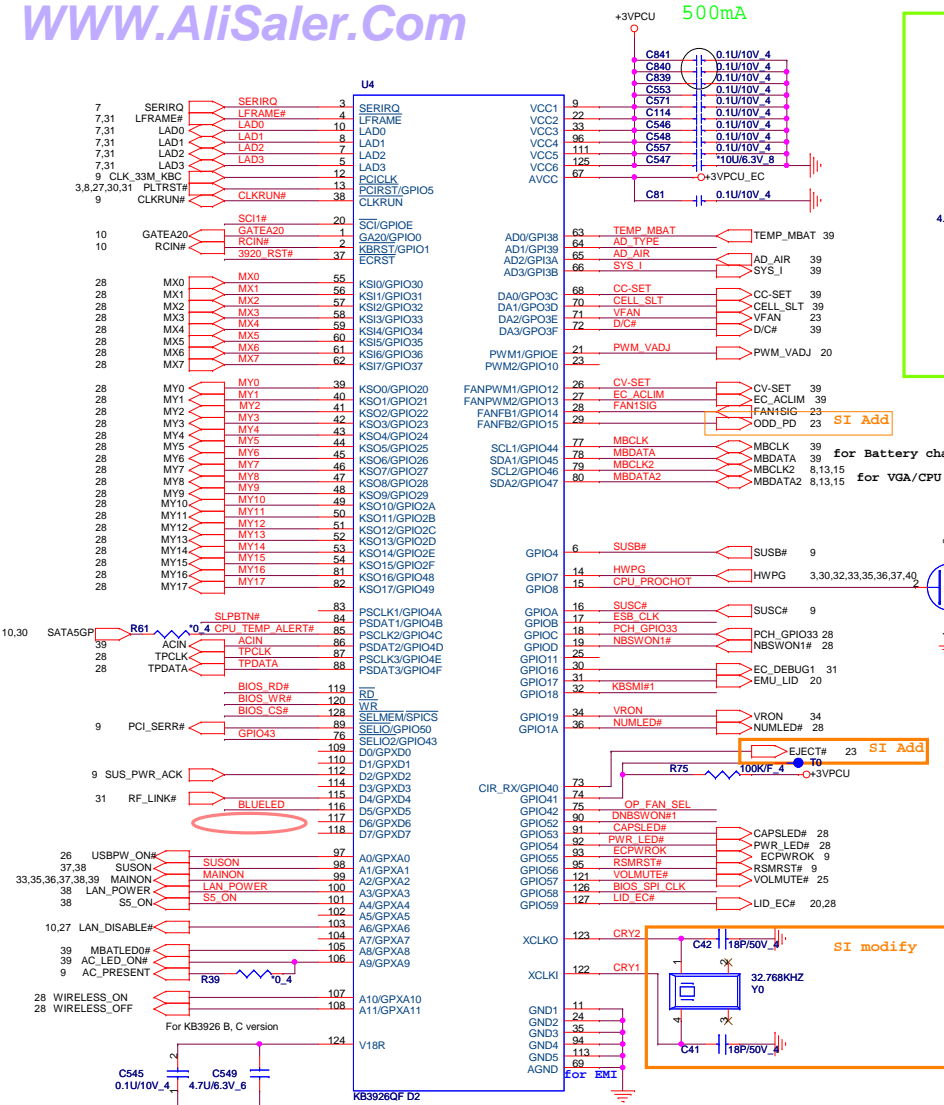


To TOUCH PAD SW board

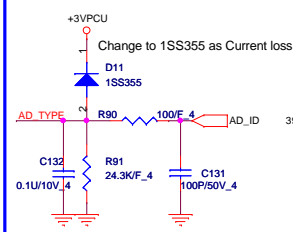


PROJECT :AX1
Quanta Computer Inc.

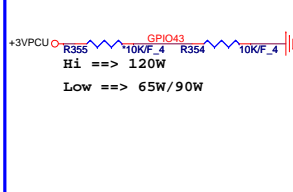
Size Custom Document Number LED/KB/SW/TP Rev 1A
Date: Thursday, November 12, 2009 Sheet 28 of 40



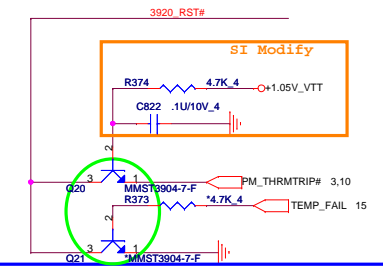
adapter Type check



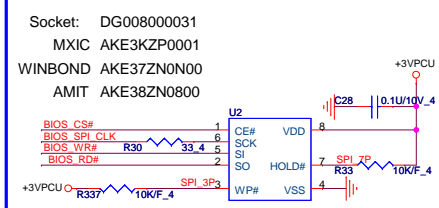
adapter select for EC



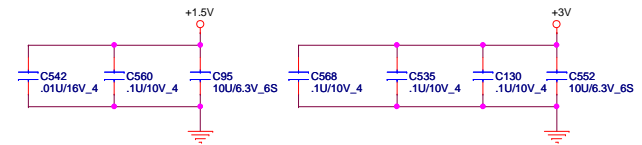
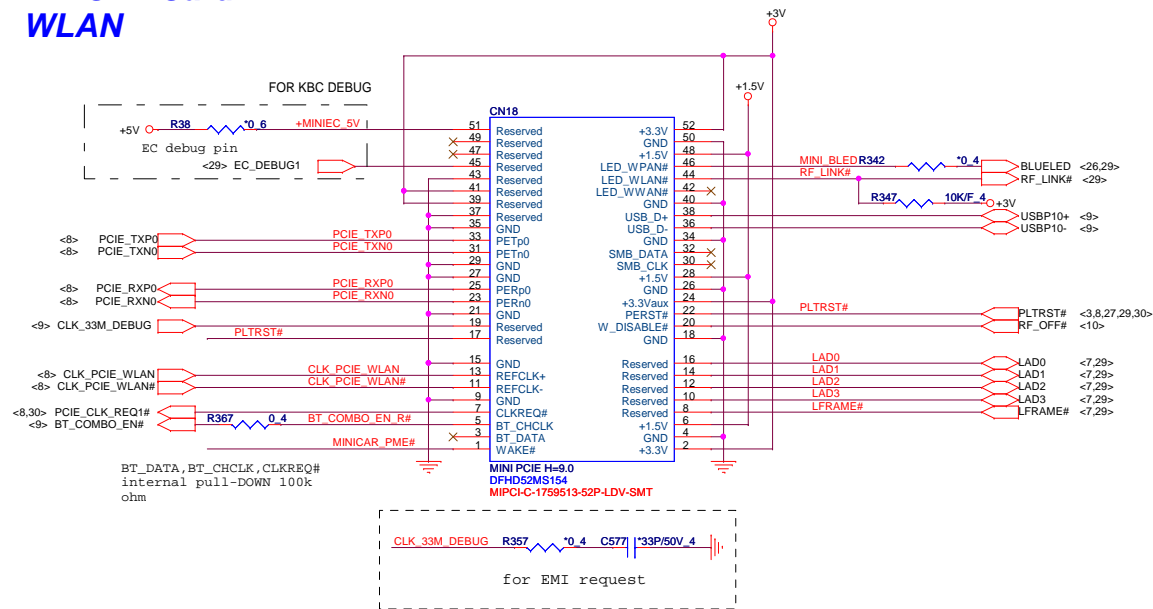
thermal shutdown circuit



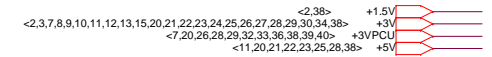
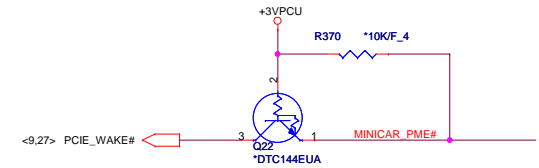
512K byte SPI EC ROM

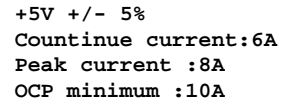






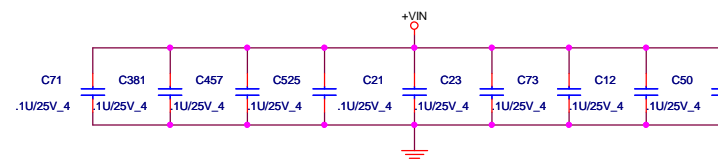
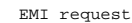
INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm



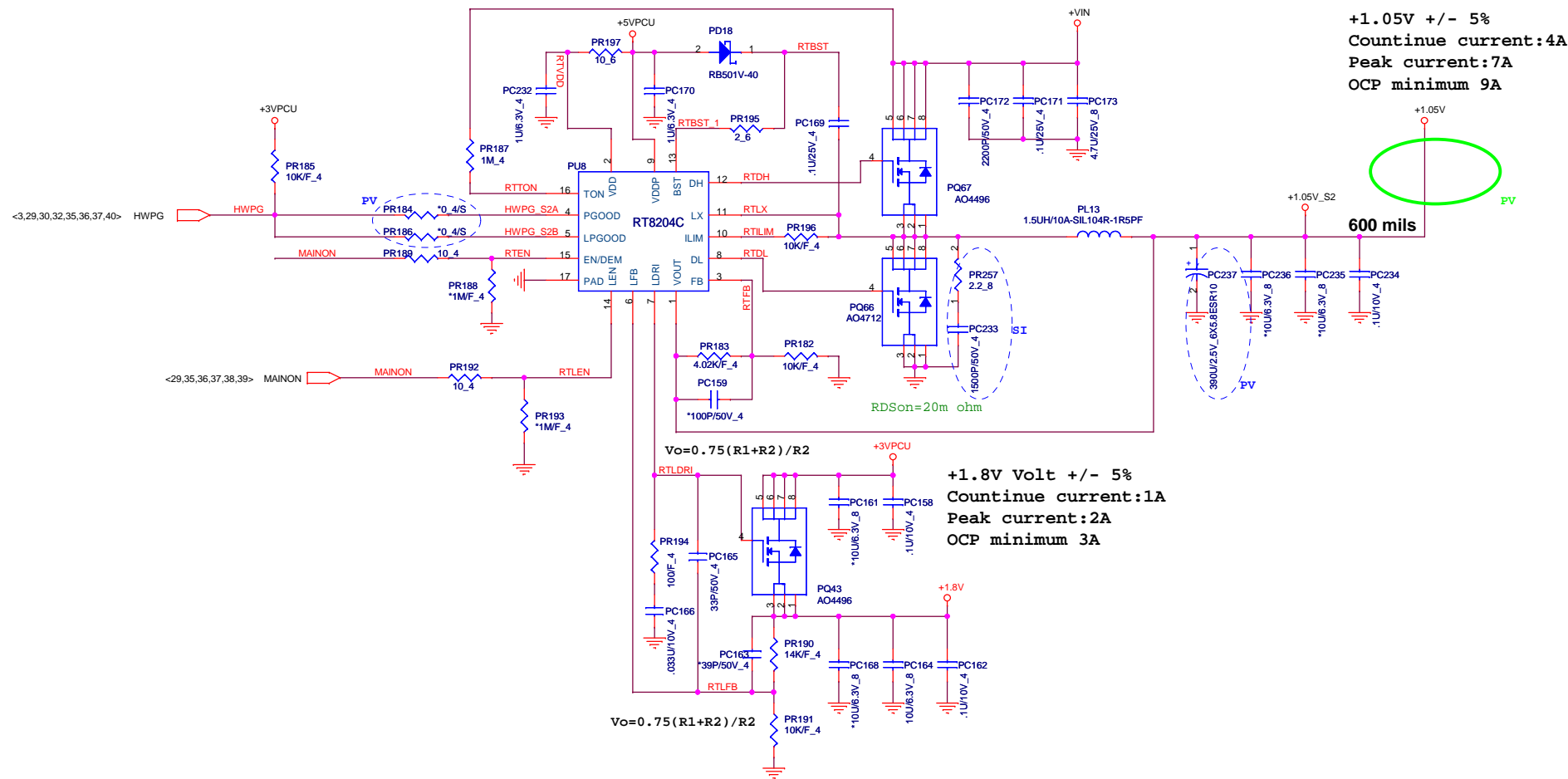


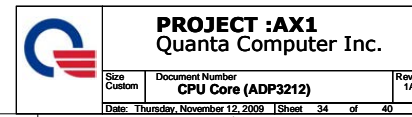
+3.3V +/- 5%
Continue current:5A
Peak current:6A
OCP minimum 7.5A

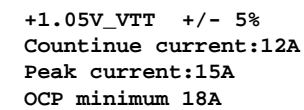
NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degreeC



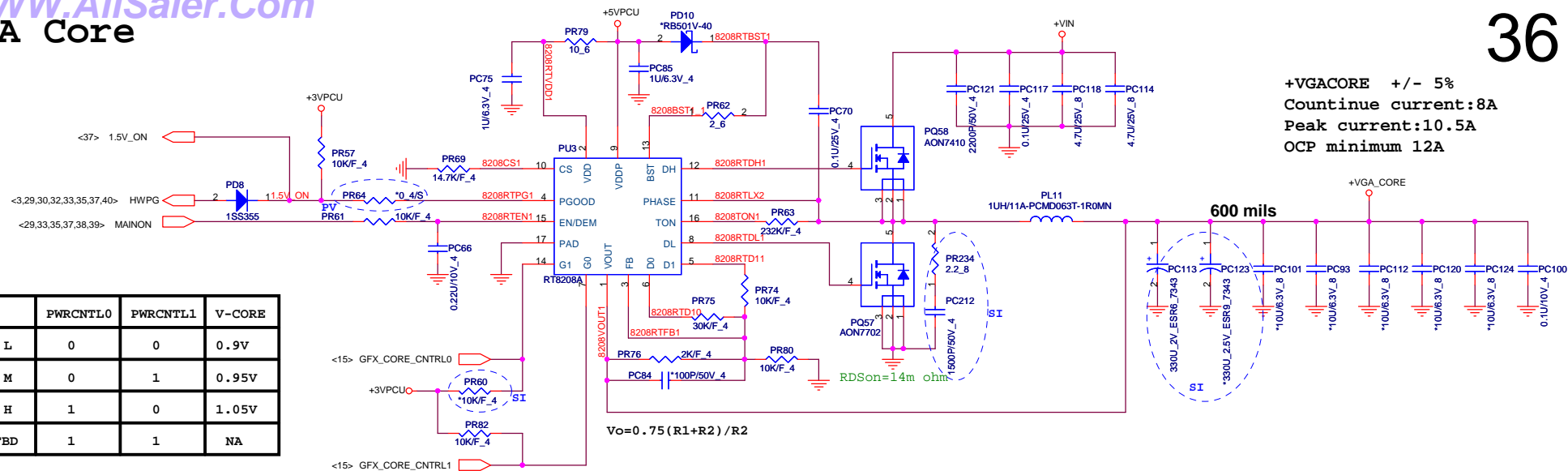
WWW.AliSaler.Com



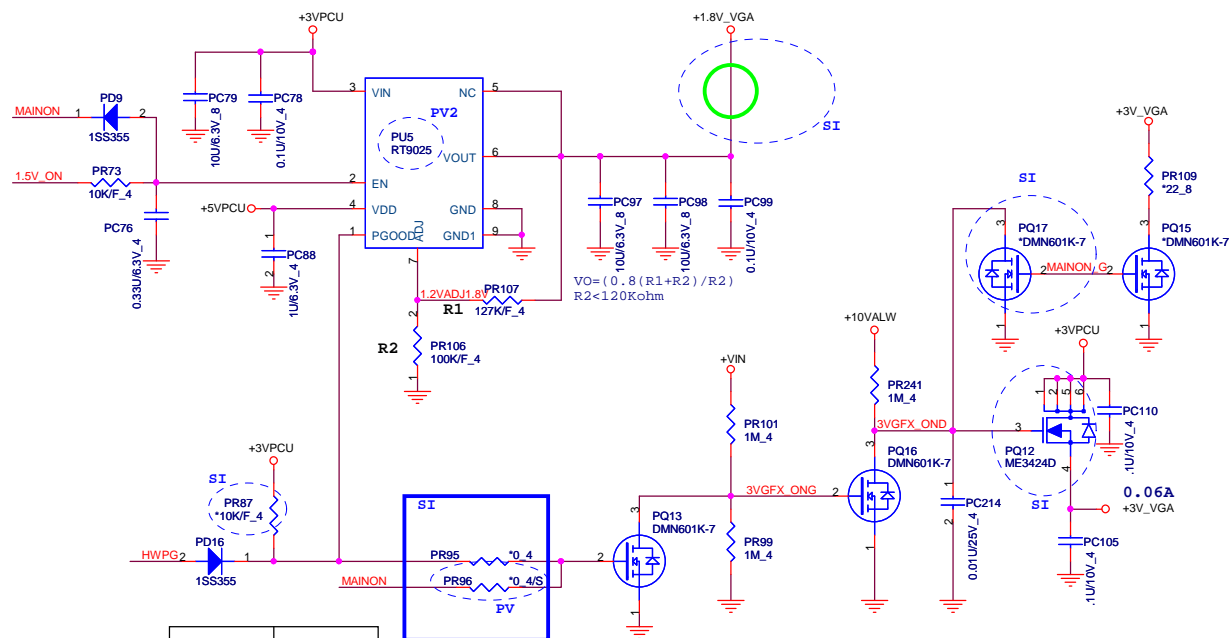




	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A

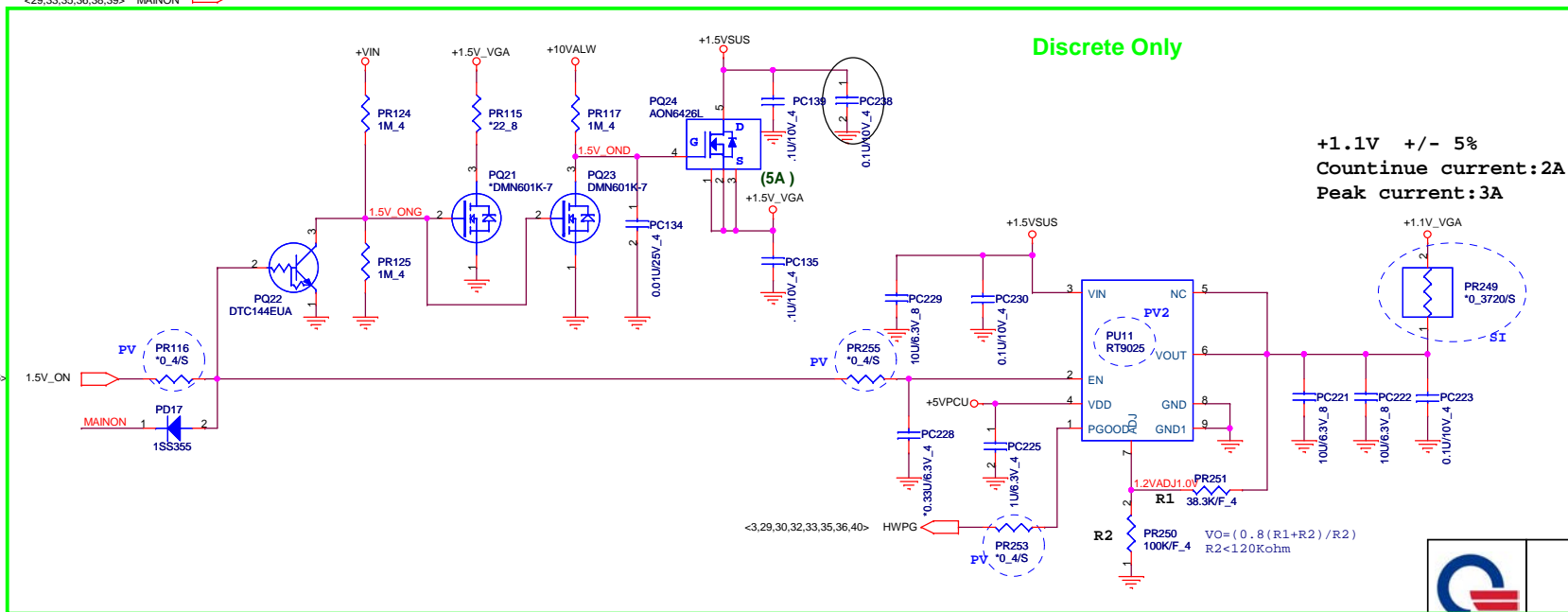


PR95	For M93
PR96	For PARK

PROJECT :AX1
Quanta Computer Inc.

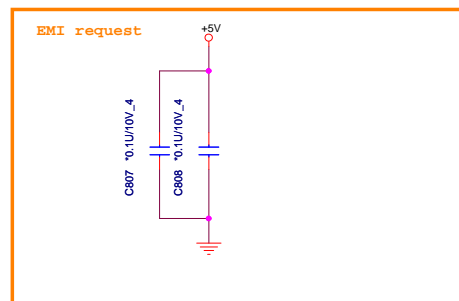
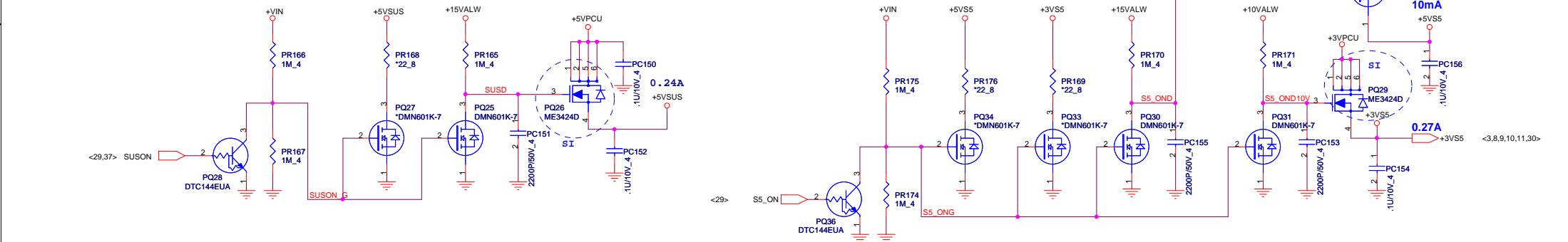
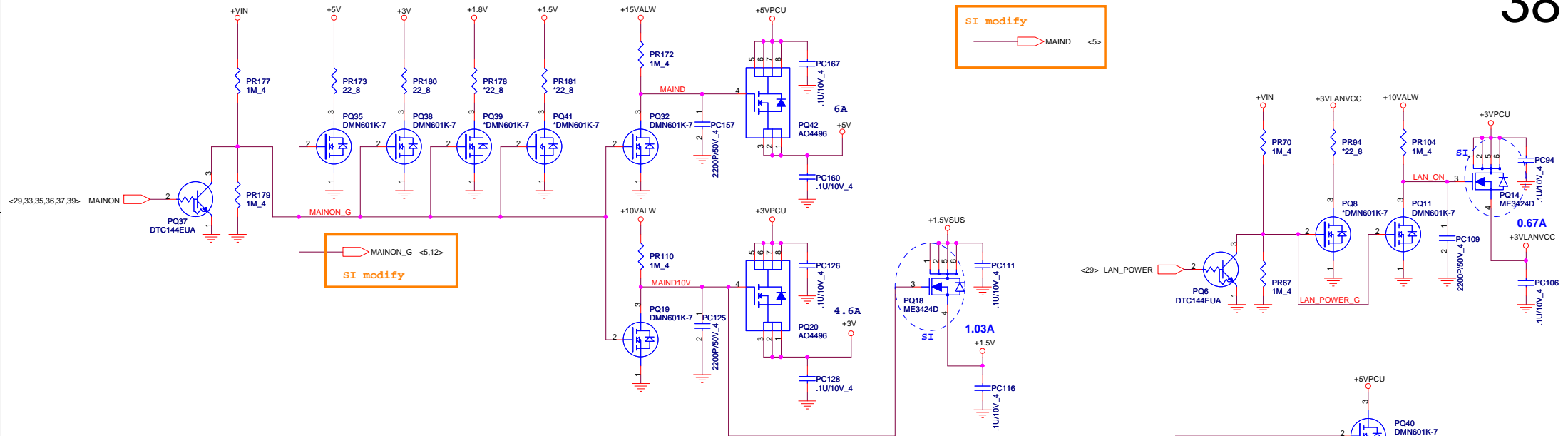
Size Custom Document Number
+VGACORE (RT8208/1.8V)


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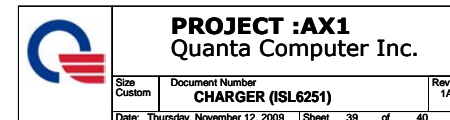


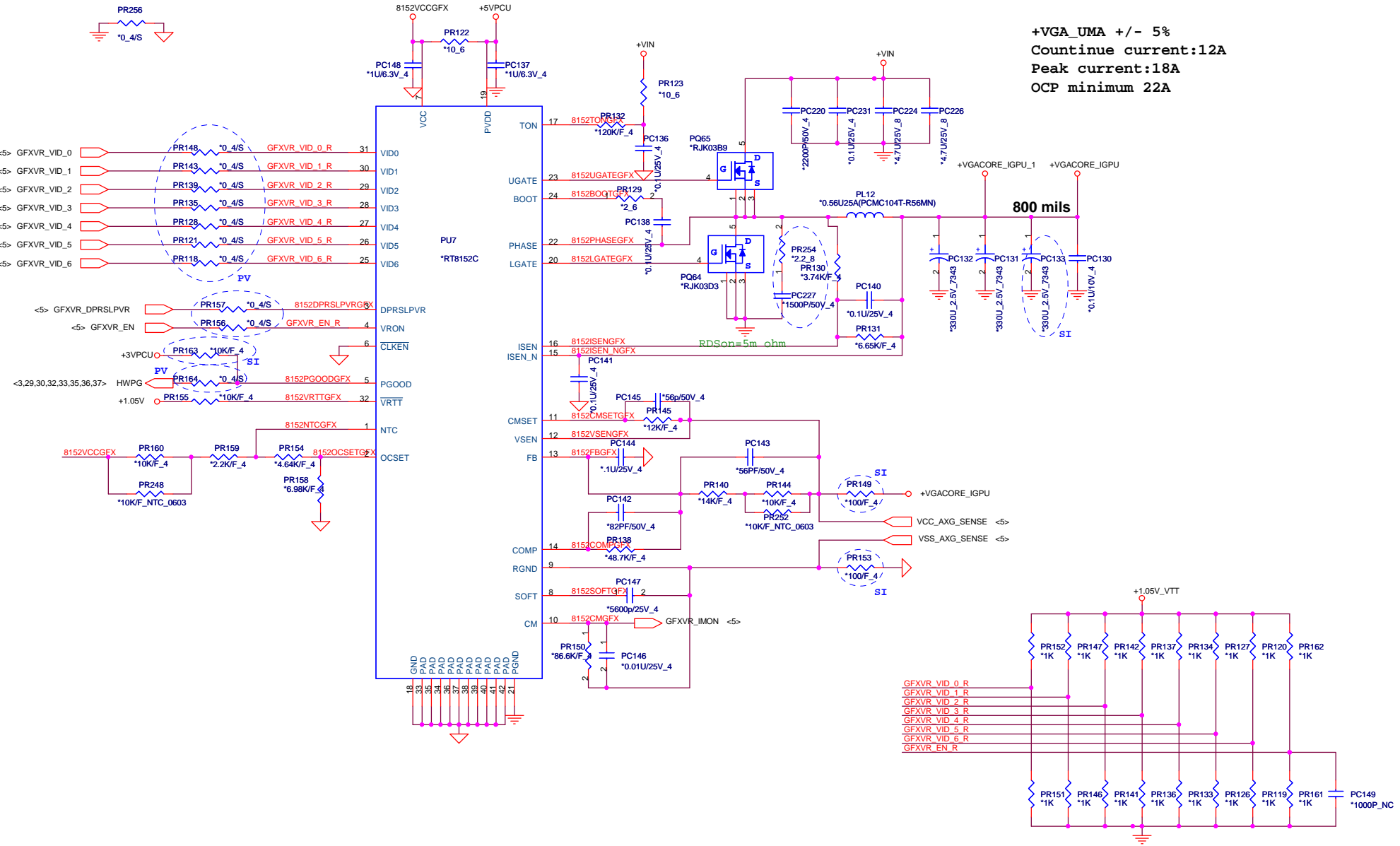
+1.1V +/- 5%
Continue current:2A
Peak current:3A

SI modify
MAIND <5>



	PROJECT :AX1 Quanta Computer Inc.		
	Size Custom Date: Thursday, November 12, 2009	Document Number DISCHARGE/3VS5/5VS5/LAN Sheet 38 of 40	Rev 1A





PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	UMA GPU CORE (RT8152C)	1A
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